COHERENT FREQUENCY SYNTHESIZER TECHNIQUES STUDY

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13 ABSTRACT

This report describes the design and operating characteristics of a pair of coherent frequency-hopped/pseudo-noise frequency synthesizers that produce a coherent 40 MHz bandwidth pseudo-noise waveform and which employ acoustic surface wave tapped delay lines as the signal-generating devices. A brief description is presented of the reason for the surface wave device implementation of the synthesizers. This presentation is followed by a detailed description of the synthesizer design. Then, a discussion follows of synthesizer testing and the results obtained. This testing revealed an RMS phase coherency between synthesizers within 0.31 radians of a perfect phase coherency, significantly better than the one radian RMS goal that had been set at the beginning of the project.

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COHERENT FREQUENCY SYNTHESIZER TECHNIQUES STUDY

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The Magnavox Company

I C

FOREWORD

The work described in this report was performed under Contract No. F30602-71-C-0197, Job Order No. 45191212, by The Magnavox Company, Government & Industrial Division, Fort Wayne, Indiana.

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EVALUATION

The significance of this report is that it documents a milestone in a program to study the application of acoustic surface wave technology to cost-effective implementation of wideband signal processing functions. The report presents the implementation of an original RADC concept for the generation of coherent frequency hopped/pseudo-noise waveforms by using acoustic surface wave multiple tap delay lines. Such a signal structure has been determined to be required for the multipurpose communication system--providing ranging, addressing and protected communications. The implementation, as described, bears out the original thinking that the acoustic surface wave approach is much simpler than conventional approaches. While reducing the complexity of such synthesizers, the measured performance of the technique shows that the high degree of coherency required between units is still achieved. The report presents detailed design information for fabricating the synthesizers and the results of the performance tests.

HENRY J. BUSH, Project Engineer

SECTION I

INTRODUCTION

The objective of the Coherent Frequency Synthesizer Techniques Study is to apply acoustic surface wave technology to the problem of generating coherent frequency-hopped/pseudo-noise waveforms. A great deal of study has been performed in recent years regarding the characteristics of waveforms required for multipurpose communications systems. The results of these studies indicate that the preferred waveforms should take the form of sideband signals composed of pseudo-noise modulated bursts of RF that hop about in frequency and which are coherent from burst to burst. Properly implemented, such a waveform would have the capability of providing multiple access to users in a communication system intended for simultaneous communications, navigation, and IFF.

A key element in such a communications system is the waveform generator (i.e., frequency synthesizer). This generator is required at the transmitting end of the system in order to generate the basic frequency-hopped/pseudo-noise (FH/PN) waveform. It is also required at the receiving end of the system in order to provide a reference signal used for demodulation of the information transmitted by the communications link. The coherency of the signal generated by such a synthesizer (i.e., its predictability) is an important characteristic, because the coherency between the transmitted and reference signals is a main factor in determining the detection efficiency of the demodulation process. It also affects the accuracy possible in the navigation (ranging) process.

Conventional implementations of coherent frequency-hopping/pseudo-noise synthesizers generally require the use of complex frequency multiplication and division techniques, mixing and filtering processes, and the generation of pseudo-noise binary sequences at a fairly high clock rate. The application of acoustic surface wave technology to the problem of generating the desired FH/PN waveforms allows the majority of the RF signal generation and pseudo-noise modulation processes, as well as the generation of the PN modulation sequences to be directly performed on the surface of acoustic surface wave devices, greatly reducing synthesizer complexity. Furthermore, by the proper choice of surface wave device materials and prudent electronic design, it is possible to fabricate synthesizers which maintain a high degree of mutual coherency.

SECTION II

SUMMARY

This report describes the design features and operating characteristics of a pair of coherent FH/PN synthesizers which employ acoustic surface wave tapped delay lines to generate a 40-MHz bandwidth pseudo-noise modulated waveform. Each synthesizer generates the waveforms by pseudo-randomly exciting a set of four surface wave device signal generators and summing the resultant outputs. The surface wave devices are designed for 40, 50, 60, and 70-MHz center frequencies and each surface wave device produces an impulse response which is comprised of a 40, 50, 60 or 70-MHz carrier biphase modulated with a 127-chip maximal length PN code. The PN code is modulated onto the carriers at a 10-MHz chip rate and, therefore, the signals produced by each surface wave device occupy a 10-MHz bandwidth. As a result, the summed output of the four surface wave devices occupies a 40-MHz bandwidth.

The synthesizers provide two modes of operation. The first mode (Mode I) produces a continuous output signal consisting of successive surface wave device impulse responses with each impulse response lasting 12.7 microseconds. The second mode of operation (Mode II) produces a 12.7-microsecond surface wave device impulse response once every 6 milliseconds. In both modes of operation, the synthesizers maintain a relative phase coherency within 18 degrees RMS of perfect (zero degrees) phase coherency at ambient temperature. For a 30°C temperature difference between synthesizers, the relative phase coherency degrades to approximately 22.5 degrees RMS.

The design techniques employed to obtain this degree of coherency and the methods employed to measure coherency are described in detail in this report. Specific recommendations are presented that discuss the incorporation of bandpass filtering, the use of an advanced quadriphase modulation technique, and the use of switchable taps on a multifunction surface wave device.

SECTION III

RATIONALE FOR SURFACE WAVE DEVICE IMPLEMENTATION OF SYNTHESIZERS

This development was undertaken with the objective of utilizing the non-dispersive delay and multitap capabilities of the acoustic surface wave tapped delay line (SWTDL) to simplify implementation of a coherent frequency-hopped/pseudo-noise synthesizer. A frequency-hopped/pseudo-noise (FH/PN) signal consists of a train of finite-length phase-modulated RF signal segments, each with a relatively wide bandwidth (typically 2 to 20 MHz).

In this particular case, each frequency segment consists of an RF carrier that is biphase modulated by a pseudo-random sequence. The composite signal is hopped in frequency in a pseudo-random manner. In addition to the pseudo-noise modulation and frequency-hopping characteristics of the composite wave form, the coherent FH/PN waveform has the characteristic that the relative phase of any one segment of the waveform is uniquely and predictably related to the relative phase of any other segment of the composite waveform.

The three characteristics of the composite waveform (frequency hopping, pseudo-noise modulation, and coherency) combine to provide mutually desirable attributes in a multifunction communication system. The frequency hopping provides resistance to narrowband and strong multiuser interference. The pseudo-noise modulation provides a degree of protection from intentional jamming, a convenient method of implementing correlation range determination, and good multipath interference rejection. Waveform coherency provides a significant improvement in range determination and also allows a communication system implementation that can approach the theoretical limits on detection efficiency.

1. CONVENTIONAL IMPLEMENTATION

Conventional techniques are available to implement coherent FH synthesizers and these can be used with shift register-generated PN sequences to synthesize coherent FH/PN signals. In many instances, however, the resulting implementation is not compatible with the faster hopping rates (75 kHz and above) nor with higher PN modulation rates (20 MHz and above).

A typical coherent FH/PN synthesizer implementation is shown in Figure 1. A stable master oscillator operating at 55-MHz is divided by 11 to provide a 5-MHz signal that is mixed with the 55-MHz signal. This produces a spectrum centered at 55 MHz with spectral lines every 5 MHz above and below 55 MHz. The spectral lines are filtered by narrowband crystal filters centered at 40, 50, 60, and 70 MHz. The 5-MHz signal obtained by dividing the 55-MHz oscillator by 11 is doubled to 10 MHz and applied to four feedback shift registers, each of which produce different 127-chip maximal length pseudo-random sequences. The four PN sequences are biphase modulated onto the filtered 40, 50, 60, and 70-MHz signals producing four phase shift keyed signals. Each occupies a 10-MHz bandwidth because of the 10-MHz PN modulation rate.

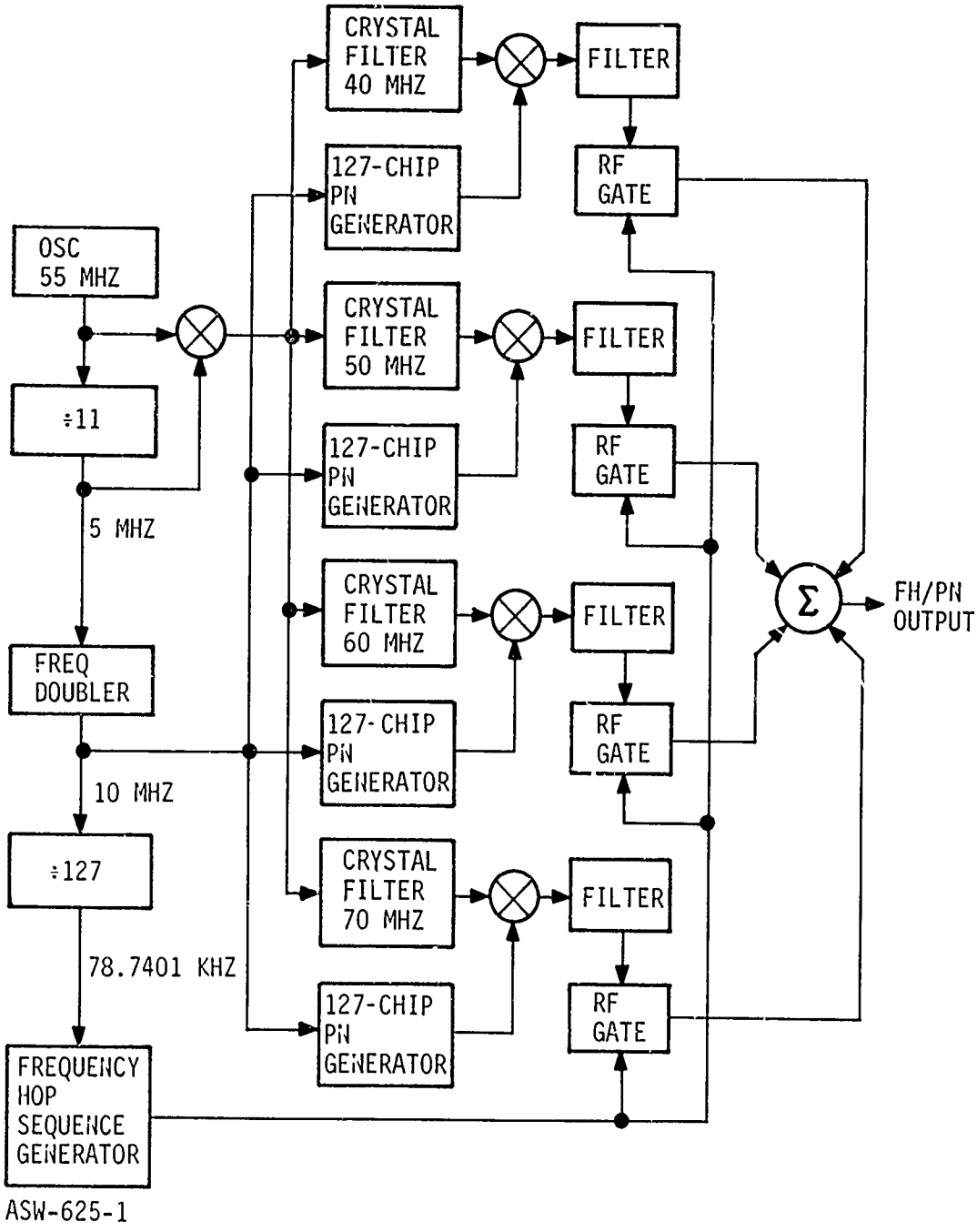

Figure 1. Conventional FH/PN Synthesizer Implementation

The modulated 40, 50, 60, and 70-MHz signals are filtered and applied to RF gates which are activated one at a time by a frequency-hop sequence generator. The frequency-hop sequence generator selects the modulated 40, 50, 60 or 70-MHz signals pseudo-randomly, thus making the frequency-hopping pseudo-random. The synthesizer output is coherent, since all frequencies and modulating signals are ultimately derived from the stable 55-MHz oscillator.

This synthesizer implementation is fairly complex as it requires frequency multiplication and division, the generation of four pseudo-random sequences at a fairly high (10 MHz) clock rate, crystal filtering of four different tones, and broadband mixing and filtering of the modulated 40, 50, 60, and 70-MHz signals. Less obvious (but nonetheless important for coherent operation) are the requirements of mutual synchronization between the four 127-chip PN sequence generators and the divide-by-11 and divide-by-127 circuits. These synchronization circuits are not indicated in Figure 1, but they are required in order to produce a predictable (and coherent) synthesizer output.

2. SURFACE WAVE TAPPED DELAY LINE CHARACTERISITCS

The coherent FH/PN synthesizer can be implemented using surface wave tapped delay lines (SWTDL's) as the signal generators. With this in mind, a brief discussion of surface wave devices is in order. Acoustic waves can be generated on the surface of any solid at frequencies extending into the gigahertz range. They propagate with no substantial frequency dispersion or attenuation, particularly on single-crystal materials. On a piezoelectric material, direct RF-to-acoustic conversion is obtained by applying electrical signals to thin film conductors deposited on a polished surface. An electrical impulse applied between thin film conductors on a piezoelectric substrate gives rise to a mechanical stress which propagates as a surface wave along the length of the substrate at approximately 3 microns per nanosecond.

This traveling wave has an electric field associated with it which extends outward from the surface. As the traveling wave propagates beneath pairs of adjacent conductors in an output transducer, it induces a voltage pulse between the conductors. These voltage pulses can be summed to provide a periodic output signal with a frequency dependent upon the wave velocity and conductor spacing, and a signal duration dependent upon the total number of conductors.

By properly arranging the conductors of an output transducer, phase reversals can be made to occur in the output signal so that a biphase-modulated signal is generated. (The phase reversals are obtained by reversing the order of the conductors in the output transducer.) If the phase reversals are arranged in a pseudo-random sequence (see Figure 2), the resultant output signal is PN modulated. Using surface wave devices with different center frequencies (and with different PN codes if desired), a FH/PN waveform can be synthesized by impulsing the surface wave devices in a pseudo-random sequence.

3. SURFACE WAVE DEVICE IMPLEMENTATION

The basic implementation of a coherent FH/PN frequency synthesizer employing surface wave devices is shown in Figure 3. A master clock provides a timing reference for the synthesizer and operates a frequency-hop sequencer. The frequency-hop sequencer controls pulser circuits used to excite four surface wave devices in a pseudo-random sequence. The surface wave devices produce signals that are centered at 40, 50, 60 or 70 MHz which are biphase modulated at a 10-megabit/second rate by 127-chip maximal length binary (PN) sequences. These signals are filtered, amplified, and summed to provide the composite FH/PN waveform. As is the case in the conventional synthesizer implementation, the composite waveform is coherent, since it is directly determined by the master clock.

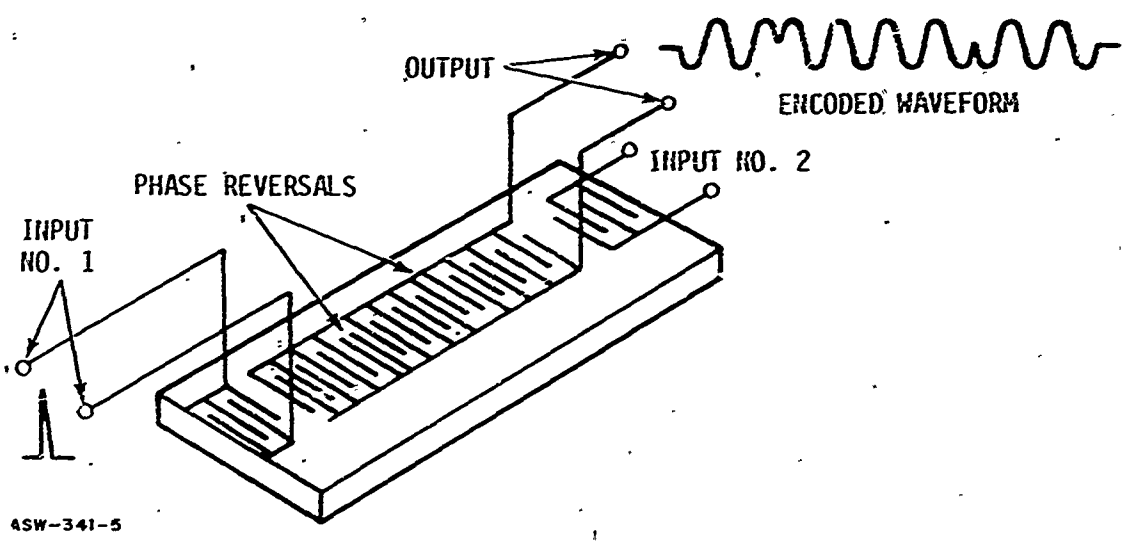

Figure 2. Surface Wave Device Signal Encoder

A comparison of this implementation with the conventional implementation reveals that the need for high-frequency divider, multiplier and synchronization circuits, crystal filters, balanced modulators, and high-speed PN sequences generators, is eliminated as all of these functions are performed simultaneously on the surface of the SWTDL substrates. Moreover, these functions are performed on a compact and rugged device that lends itself to potentially low cost and repeatable high-volume production.

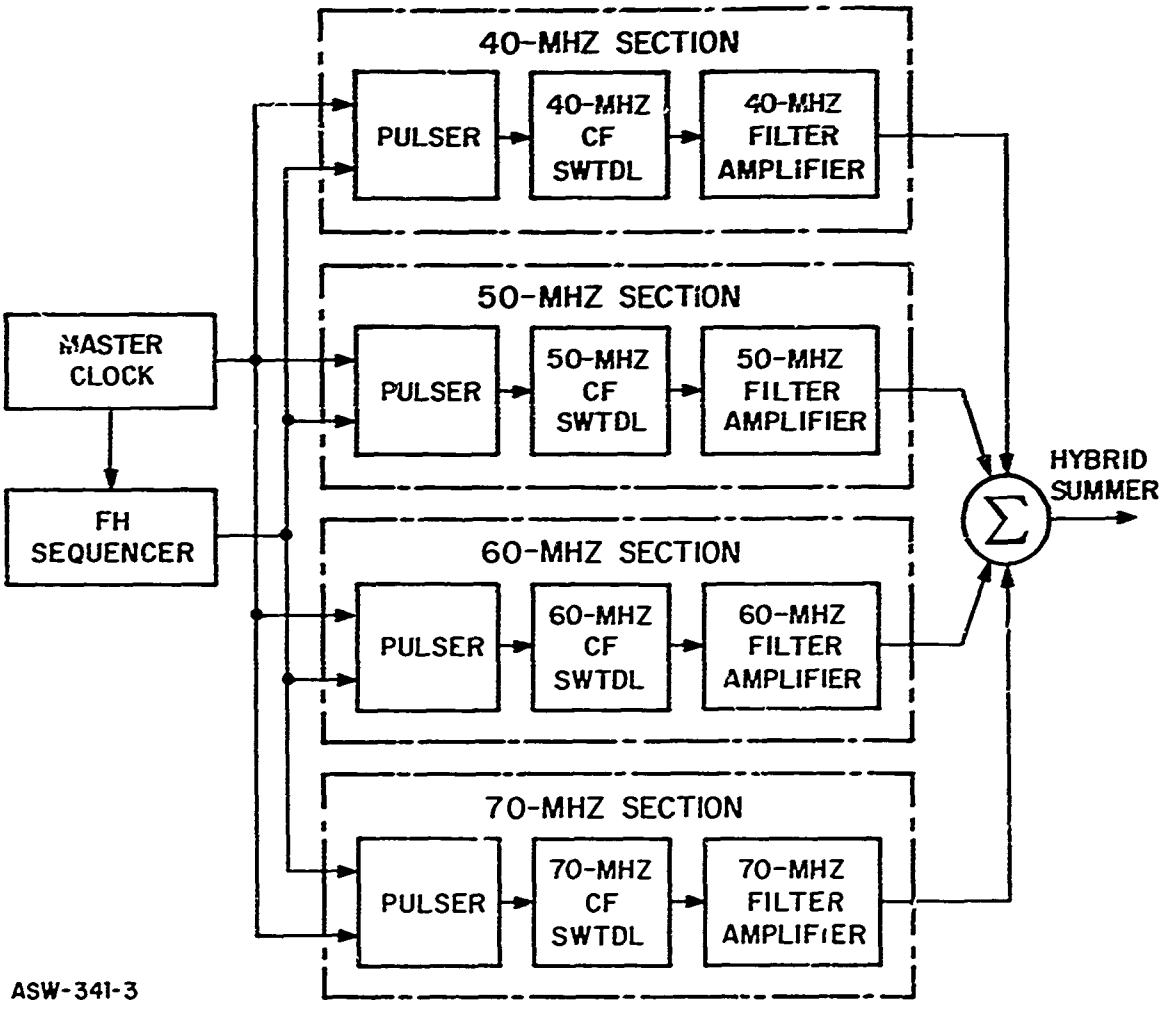

Figure 3. Surface Wave Device FH/PN Synthesizer

SECTION IV

SYNTHESIZER DESIGN PARTICULARS

1. GENERAL OPERATION

The two synthesizers are referred to as synthesizer No. 1 and synthesizer No. 2 in this report. Although the techniques used to generate the FH/PN output signals are identical in both synthesizers, there are slight differences in the synchronization circuitry between the synthesizers and, hence the synthesizer No. 1, synthesizer No. 2 distinction is made.

Synthesizer No. 1 may be considered as the "transmitting" synthesizer. In addition to its FH/PN output, it produces PN frequency-hop, pulser clock and system clock synchronization signals. Synthesizer No. 2 may be considered as the "receiving" synthesizer. It produces a FH/PN output similar to that of synthesizer No. 1. In addition, it accepts the PN frequency-hop, pulser clock and system clock synchronization signals from synthesizer No.1 and uses these signals to synchronize its FH/PN output with the FH/PN output from synthesizer No. 1. The techniques used to achieve synchronization are discussed in greater detail later on in this report.

A functional block diagram of synthesizer No. 1 is shown in Figure 4 and a similar block diagram of synthesizer No. 2 is shown in Figure 5 to illustrate FH/PN and synchronization signal flow paths. Referring to Figure 4, a 10-MHz clock is generated by an oven-stabilized 10-MHz crystal oscillator. The oscillator produces a TTL logic compatible square wave which is fed to a frequency-divider circuit. The frequency-divider circuit divides the 10-MHz clock by 127 for Mode I (continuous output) operation, and by 60,000 for Mode II (6-millisecond periodic) operation. The resultant output of the frequency-divider circuit is selected by the Mode switch, (switch S1) depending upon the mode of operation of the synthesizer. The selected output will hereafter be referred to as pulser clock.

a. Mode I Operation

In Mode I operation, the divide-by-127 output of the frequency divider circuit is selected for pulser clock. In this mode, pulser clock is an approximately 100-nanosecond wide pulse with a 12.7-microsecond period, (78.7401 kHz repetition rate). Pulser clock is fed to the frequency-hop sequence generator and the frequency-hop sequence generator develops the pseudo-random frequency-hopping sequence. The frequency-hopping sequence is synthesized from a 63-chip maximal length pseudo-random code generated by the frequency-hop sequence generator and is clocked at the 78.7401 kHz pulser clock repetition rate.

The frequency-hop sequence generator produces four SWTDL enable signals corresponding to the 40, 50, 60, and 70-MHz SWTDL center frequencies. The enable signals occur sequentially in a manner determined by the pseudo-random frequency-hopping sequence. Thus, during any one 12.7-microsecond pulser clock period, only one of the four SWTDL enable signals is logically true.

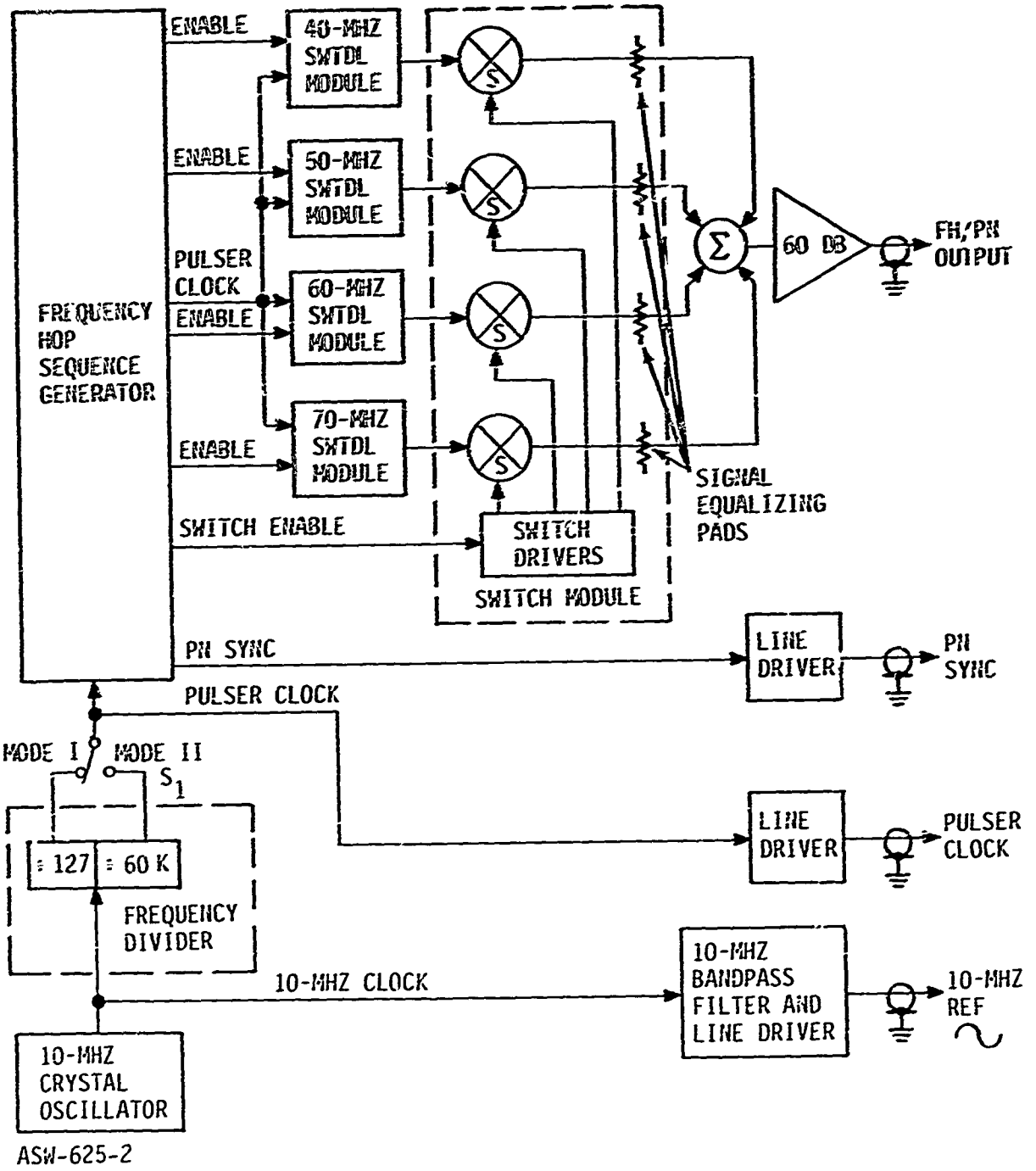

Figure 4. Synthesizer No. 1 Block Diagram

Each SWTDL enable signal is fed to its corresponding SWTDL module, while pulser clock is fed to all four SWTDL modules simultaneously. Each SWTDL module contains a SWTDL pulser and each pulser logically AND's its enable signal and the pulser clock signal. When a SWTDI enable and pulser clock signal occur simultaneously, the enabled

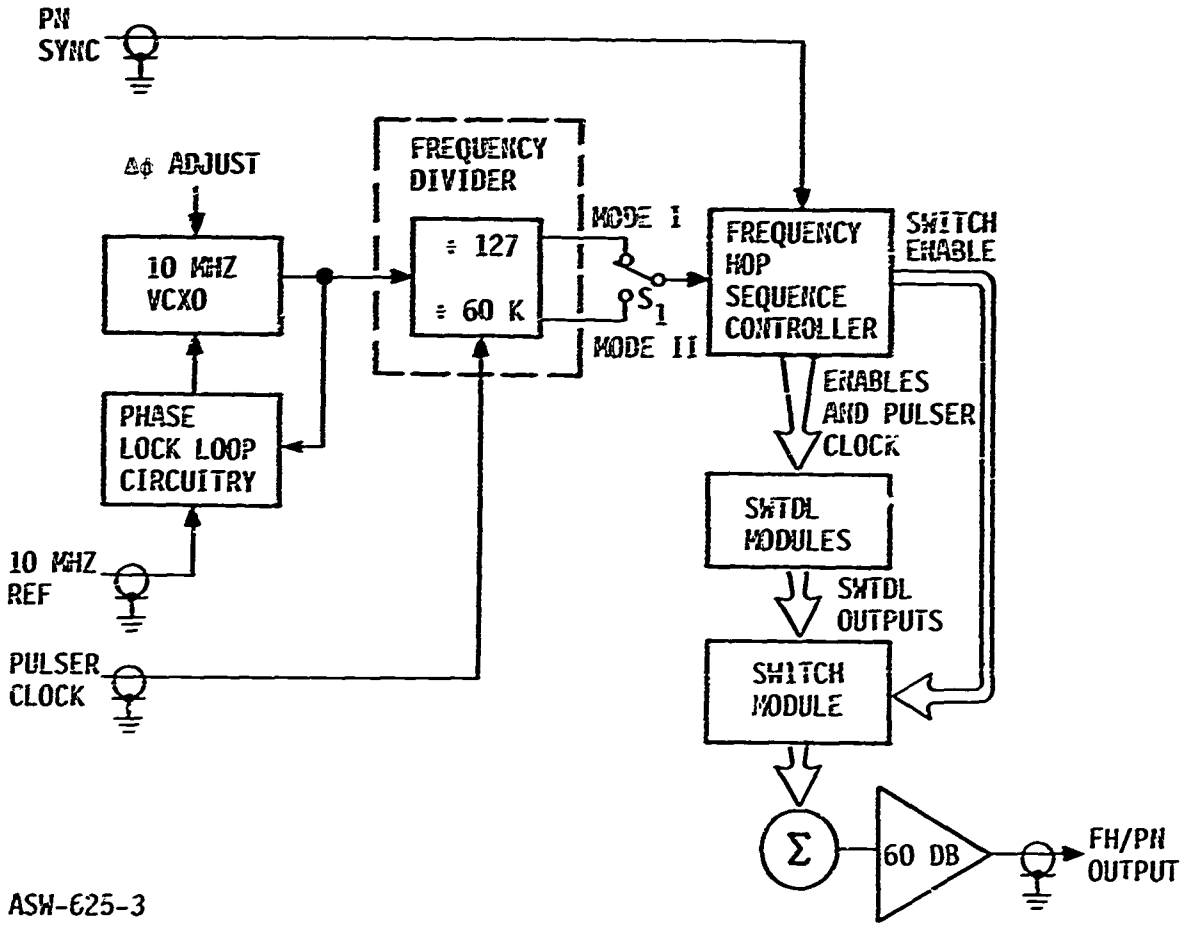

Figure 5. Synthesizer No. 2 Block Diagram

pulser excites its corresponding SWTDL. Since the Mode I pulser clock repetition rate is 78.7401 kHz, a new SWTDL is enabled every 12.7 microseconds and pulsed in accordance with the frequency-hopping pattern. Each SWTDL produces an impulse response precisely 12.7 microseconds long when excited. Thus, in Mode I operation an impulse response is always occurring, since the pulser clock period is 12.7 microseconds

The output of the SWTDL modules is fed to the switch module. The switch module contains four RF switches used to gate the appropriate SWTDL module output to the synthesizer summing circuitry. The RF gating improves the signal-to-noise ratio at the synthesizer output. (This is discussed in more detail later in this report). The frequency-hop sequence generator provides the switch module with four switch enable signals. The switch enable signals are identical to the SWTDL module enable signals, but are delayed in time approximately 4.9 microseconds to compensate for the 4.9 microseond delay between the excitation of a SWTDL input transducer and the start of a SWTDL impulse response. (The delay arises from the physical separation of the SWTDL input and output transducers).

The output of the RF switches is fed to signal equalizing pads which appropriately attenuate the four SWTDL outputs such that the signals fed to the power summer are of equal amplitude. Thus, the output of the summer is a continuous FH/PN signal composed of equal amplitude, 12.7 microsecond long impulse responses that are hopped in frequency by the pseudo-random frequency-hopping sequence. This signal is fed to an output amplifier which provides 60 dB of wideband gain. The amplifier output level is approximately -5 dBm into 50 ohms and it is fed to a BNC connector on the synthesizer chassis.

Synthesizer No. 1 produces three synchronization signals for use in synthesizer No. 2, namely PN sync, pulser clock, and system reference clock. Pulser clock, taken directly from the output of the frequency-divider circuit, is supplied to a line driver and fed to a chassis BNC connector. System clock (the 10-MHz reference) is obtained by filtering the square wave output of the 10-MHz crystal oscillator in synthesizer No to obtain a 10-MHz sine wave. This signal is supplied to a line driver and then to a chassis BNC connector. (A 10-MHz sine wave is required in order to operate the 10-MHz phase lock loop in synthesizer No. 2). PN sync is derived from the frequency-hop sequence generator. The frequency-hop sequence generator is a six-stage feedback shift register that generates the 63-chip frequency-hop sequence. The logical state of the six stages (i.e., flip-flops) in the shift register are continuously monitored and a particular point in the 63-chip sequence (which only occurs once per 63-chip sequence) is digitally detected by observing the states of the six flip-flops. When this condition is recognized, a (PN sync) pulse is generated and fed to a line driver and then to a chassis BNC connector.

The 10-MHz reference signal is fed to synthesizer No. 2 where it is used as the reference signal in a 10-MHz phase lock loop. Synthesizer No. 2 contains a 10-MHz voltage-controlled crystal oscillator (VCXO) which drives the frequency-divider circuit in synthesizer No. 2. The phase lock loop circuitry filters the VCXO output, obtaining a 10-MHz sine wave and compares the phase of this signal with the 10-MHz reference signal from synthesizer No. 1. The error signal produced by the phase lock loop circuitry is used to control the frequency of the VCXO. Therefore, the 10-MHz clocks in synthesizers No. 1 and No. 2 are maintained coherent. The relative phase of the VCXO signal is made adjustable by means of a "ϕ adjust" control so that relative phase of the synthesizer No. 1 and No. 2 clocks can be varied for experimental purposes.

The 10-MHz clock produced by the VCXO drives the frequency-divider circuit in synthesizer No. 2 which in turn produces synthesizer No. 2 pulser clock. In order for synthesizers No. 1 and No. 2 to be coherent, their pulser clocks must be coherent. Therefore, the pulser clock signal from synthesizer No. 1 is compared with the pulser clock in synthesizer No. 2. If the synthesizer No. 1 and No. 2 pulser clocks are not occurring simultaneously, 10-MHz clock pulses fed

to the synthesizer No. 2 frequency-divider circuit are deleted until the synthesizer No. 1 and No. 2 pulser clocks synchronize.

Once the synthesizer No. 1 and No. 2 10-MHz clocks and pulser clocks are synchronized, the frequency-hopping sequence of synthesizer No. 2 must be synchronized to the hopping sequence of synthesizer No. 1. As mentioned previously, the PN sync pulse from synthesizer No. 1 occurs when a particular state of the six flip-flops comprising the frequency-hopping sequence generator in synthesizer No. 1 is recognized. The PN sync pulse fed to synthesizer No. 2 forces the state of the six flip-flops in the synthesizer No. 2 frequency-hopping generator to be identical to that of the hopping sequence generator in synthesizer No. 1, thereby synchronizing both sequence generators. Once this occurs, both synthesizers are frequency-hopping in unison and the two synthesizer outputs are therefore coherent.

b. Mode II Operation

In Mode II operation, the mode switch (shown schematically as S1 in Figures 4 and 5) selects the divide-by-60,000 output of the frequency-divider circuit. Therefore, the pulser clock is an approximately 100-nanosecond wide pulse with a 6-millisecond period (166.666 Hz repetition rate). As a result, the frequency-hop sequence generator selects and excites a new SWTDL every six milliseconds. The frequency-hopping sequence is the same as in the Mode I case. Since the impulse response of each SWTDL is 12.7 microseconds, the synthesizer output is comprised of a 12.7 microsecond burst of RF every six milliseconds and the center frequency of each successive burst hops in the same manner as in Mode I operation. With the exception of the frequency-hopping rate, the operation of the synthesizers (including the synchronization techniques), is the same in Mode I and Mode II.

2. SWTDL DESIGN

a. Substrates

All of the surface wave tapped delay lines used in the synthesizers are fabricated on ST-cut Quartz substrates. ST-cut Quartz was selected for the substrate material, because it has several desirable characteristics relative to some of the other commonly used piezoelectric materials such as lithium niobate or bismuth germanium oxide. ST Quartz has a very small surface wave velocity temperature coefficient and hence a small time delay temperature coefficient. Therefore, the waveforms produced by ST Quartz SWTDL's tend to be stable with temperature. This is especially important when considering the coherency between two synthesizers that have to operate in different temperature environments.

Quartz has a much lower electrical/acoustic coupling coefficient than either lithium niobate or bismuth germanium oxide. While this means that a Quartz SWTDL has a larger insertion loss than SWTDL's fabricated

on lithium niobate or bismuth germanium oxide, it also means that a much lower (and usually insignificant) level of spurious signals is generated by a Quartz delay line.

The SWTDL substrates used in the synthesizers are 4 inches long by ½ inch wide by 1/8 inch thick. They were all cut with a 42.75-degree Y-axis rotation, (ST-cut), and oriented such that the long edge of the subtrate corresponds to within 5 minutes of the "X" crystallographic axis. One surface (X, rotated Y) was polished to a one micron (or better) finish. A layer of aluminum, approximately 2000 angstroms thick, was then vacuum-evaporated onto the polished surface of the substrates to serve as the metallization for the interdigital transducer patterns.

b. Transducer Patterns

The transducer patterns on each SWTDL consist of four input transducers (2 on each end of the device) and an output transducer. The transducer pattern for the 40-MHz SWTDL is shown in Figure 6 (input transducers were placed on each end of the devices so that the devices could be used as signal generators or as parallel correlating matched filters). Two input transducers were placed on each end of the devices so that damage to one transducer would not render the device useless.

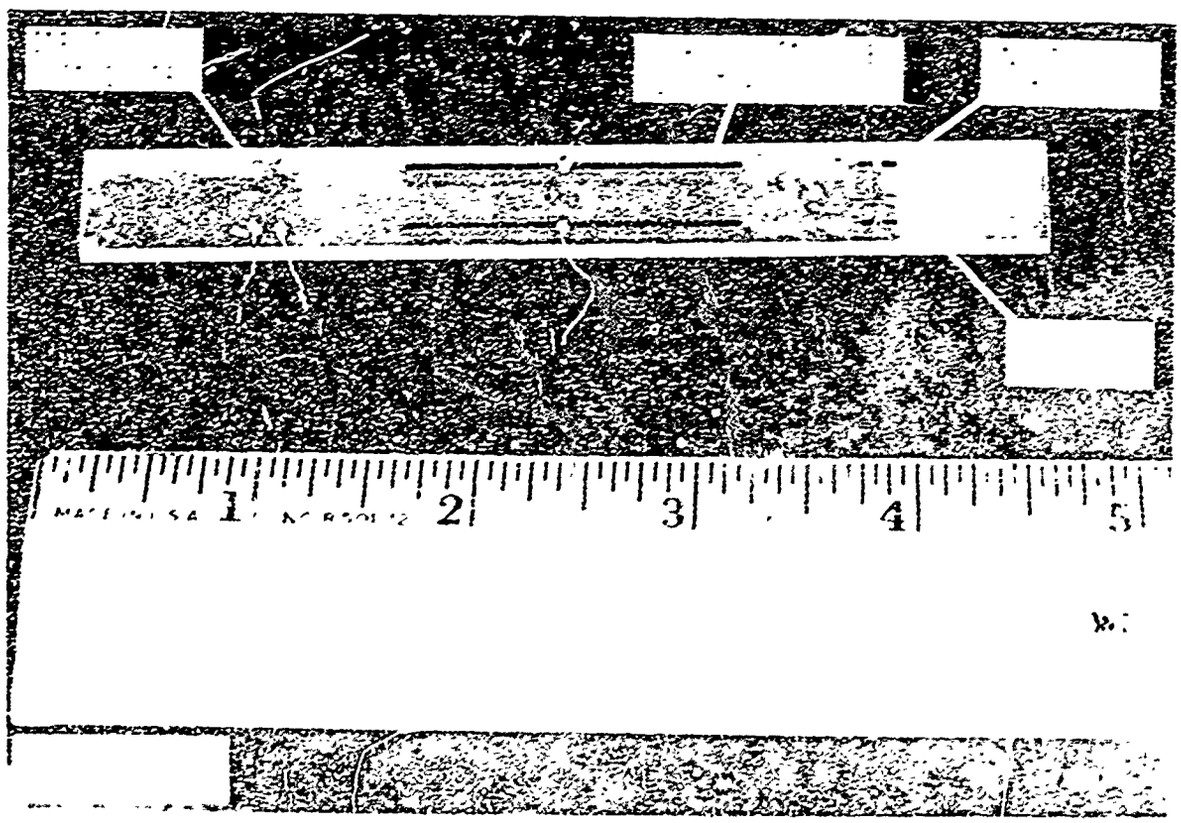

Figure 6. 40-MHz SWTDL

The initial design of the 40-MHz SWTDL pattern consisted of n=4 pair input transducers and n=4 pair per tap output transducers. In this instance, the theoretical acoustic bandwidth of the input transducers and of each tap of the output transducer was 10 MHz. Therefore, the composite input transducer/output transducer acoustic bandwidth was approximately 6.4 MHz. As a result, the impulse response of the device exhibited significant amplitude modulation due to bandlimiting.

In order to alleviate this problem, the number of pairs per tap on the output transducer was changed from four pair to one pair with the result that the acoustic bandwidth of the device was essentially determined by the bandwidth of the input transducer (10 MHz). The effect of this change was that the amplitude of the device's impulse response was essentially constant and the frequency spectrum exhibited a $\left(\frac{\sin x}{x}\right)^2$ shape with nulls at 30 and 50 MHz.

The design of the 50, 60, and 70-MHz SWTDL's was made similar to that of the 40-MHz SWTDL. In each case, the input transducer was designed for a 10-MHz acoustic bandwidth while the output transducers consisted of single interdigital pairs per tap. A synopsis of the transducer design characteristics for the 40, 50, 60, and 70-MHz SWTDL's is given in Table I.

TABLE I. SWTDL TRANSDUCER CHARACTERISTICS

	Center Frequency			
	40 MHz	50 MHz	60 MHz	70 MHz
Number of pairs in Input Transducers	4 pairs	5 pairs	6 pairs	7 pairs
Output Transducer	127 taps (1 pair/tap)	127 taps (1 pair/tap)	127 taps (1 pair/tap)	127 taps (1 pair/tap)
Interdigital Finger Spacing, $\lambda/2$	1.554 mills	1.243 mills	1.036 mills	0.888 mills
Output Transducer Tap Spacing	12.432 mills	12.432 mills	12.432 mills	12.432 mills
Interdigital Finger Overlap	233.1 mills	186.5 mills	155.4 mills	133.2 mills

c. SWTDL Codes

Each SWTDL output transducer contains a 127-chip maximal length pseudo-random code and a different code is used on each SWTDL. A computer search was made of the 18 maximal length codes available (from the family of all possible 127-chip codes), and four codes with mutual cross-correlations of less than 25/127 of the individual code auto-correlations were selected. The code number, characteristic equation and initial conditions of each of the four codes is summarized in Table II.

TABLE II. SWTDL PN CODES

Center Frequency	Code Number	Characteristic Equation
40 MHz	211	$P(X) = X^7 + X^3 + 1$
50 MHz	217	$P(X) = X^7 + X^3 + X^2 + 1$
60 MHz	277	$P(X) = X^7 + X^5 + X^4 + X^3 + X^2 + X + 1$
70 MHz	323	$P(X) = X^7 + X^6 + X^4 + X + 1$
Initial Conditions are 1000000 for All Codes.		

d. SWTDL Matching

Bandpass matching of the SWTDL output transducers was employed to maximize the SWTDL output signal levels so as to provide a good signal-to-noise ratio at the synthesizer output. In addition, the matching provides a degree of bandpass filtering of the SWTDL outputs and reduces any out-of-band spurious signals that might exist. The technique chosen was to match the output impedance of each SWTDL output transducer to 50 ohms (the characteristic impedance of all the non-surface wave RF components used in the system).

The basic matching network employed for each SWTDL output transducer is shown in Figure 7. It is a tapped parallel tank circuit composed of the equivalent shunt capacitance of the output transducer, C_T, and a tapped variable inductor, L. The tank is shunted by the equivalent shunt output resistance of the output transducer, r_T, and by the equivalent resistance, r_p, of the circuit's 50-ohm load that is stepped up by the tapped inductor.

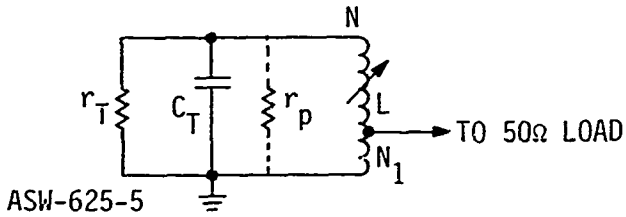

Figure 7. SWTDL Output Matching

The 3 dB bandwidth of this network is determined by its loaded Q, (Q_L) and resonant frequency f_o (i.e., 3 dB bandwidth = fo/Q_L). The loaded Q is $Q_L = r'_p/2\pi f_o L$, where r'_p is the parallel equivalent of r_p and r_T. Each matching network was designed for a 3 dB bandwidth of 20 MHz in order to avoid any significant amount of phase distortion in the 10-MHz bandwidth of the SWTDL outputs. The characteristics of each matching network are summarized in Table III. Using this matching technique, the output power of each SWTDL was increased 6 dB relative to the output power obtained when no matching was employed.

TABLE III. SWTDL OUTPUT MATCHING NETWORK CHARACTERISTICS

	Center Frequency			
	40 MHz	50 MHz	60 MHz	70 MHz
Loaded Q,	2.0	2.5	3.0	3.5
C_T*	29.3 p_f	24.0 p_f	19.2 p_f	17.0 p_f
r_T	1.2K Ω	1.7K Ω	2.1K Ω	2.4K Ω
L	0.5 μh	0.36 μh	0.38 μh	0.3 μh
r'_p	270 Ω	325 Ω	420 Ω	490 Ω
Total** Turns, N	8.0	6.5	6.75	6.25
Tapped at Turn, N_1	3.5	2.5	2.3	2.0

* C_T represents the shunt capacitance of the output transducer plus the stray capacitance caused by the output leads.

** Inductor L is wound on a Cambion coil form, Part No. 3652-7. The tap is referenced from the ground side of the inductor.

3. PULSERS

The pulser circuits used in the synthesizers produce narrow baseband pulses which are used to excite the SWTDL's. Each pulser consists of a pulse generator and pulse amplifier and each SWTDL has its own pulser. A schematic diagram of the basic pulser circuit is shown in Figure 8a. The pulse generator consists of a high-speed inverter Z_1 and a high-speed NAND gate Z_2. When the pulser is enabled by a logic level from the frequency-hop sequence generator, the A-input to Z_2 is high. When pulser clock occurs, the B-input to Z_2 sees a transition from high to low that lasts approximately 100 nanoseconds, (see Figure 8b). This pulse is also fed to inverter Z_1 and the output of Z_1 is fed to the C-input of Z_2. The output of Z_1 is delayed by T_d seconds as a result of the propagation delay of Z_1. Thus, the B and C inputs of Z_2 overlap each other by T_d seconds and as a result, the B and C inputs to Z_2 are both high for a time T_d as shown in Figure 8b. If the A-input of Z_2 is enabled during this time, Z_2 produces an output pulse (D in Figure 8b) that is T_d seconds wide. If the A-input to Z_2 is not enabled, Z_2 does not produce an output pulse.

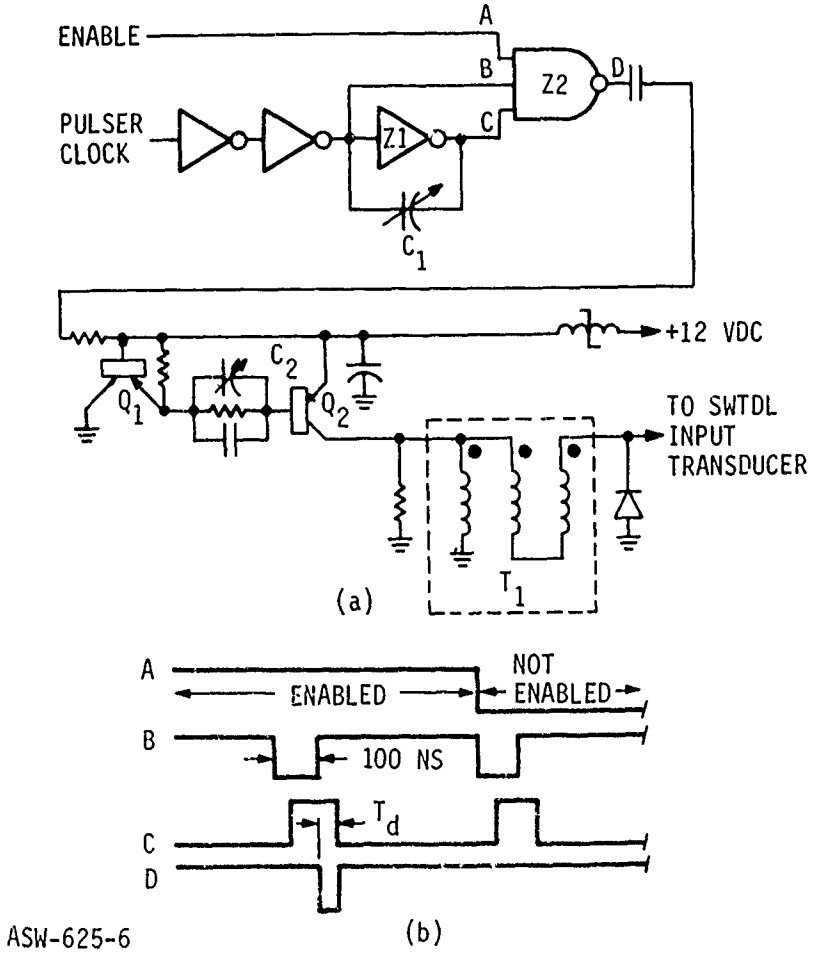

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Figure 8. Schematic of Basic Pulser Circuit

The width of the pulses produced by the pulse generator is determined by the propagation delay of Z_1. Since pulse widths on the order of 10 nanoseconds were required to excite the SWTDL's, Schottky clamped TTL inverters were used for Z_1. Specifically, a Texas Instruments, Type SN74S04 inverter, was used as this device exhibits a propagation delay of approximately 5 nanoseconds. The width of the pulse was made adjustable by means of a feed-around capacitor C_1. The pulser clock input to Z_1 was buffered by two additional Schottky clamped inverters in order to eliminate the loading effect of capacitor C_1, since pulser clock feeds all four SWTDL pulsers simultaneously.

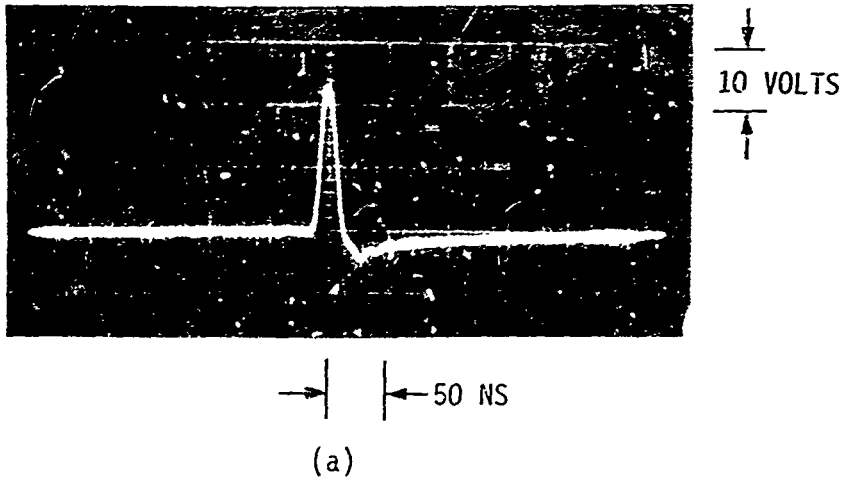
The output of Z_2 is a 5-volt logic level transition This signal is amplified by a pulse amplifier comprised of Q_1 and Q_2. High-speed switching transistors were used for Q_1 and Q_2 (2N4260's) in order to preserve the rise and fall edges of the Z_2 output. The output of Q_2 is a positive going pulse with an amplitude of approximately 8 volts. The shape and amplitude of the pulse was made adjustable by means of the speed-up capacitor C_2.

In order to obtain the largest possible output from each SWTDL, an autotransformer was used to increase the amplitude of the Q_2 output pulse, (T_1 of Figure 8). This transformer is comprised of an 8-turn trifilar winding on an Indiana General CF-102-Q3 toroid core. An approximate voltage step-up of three is obtained with this transformer with a resultant increase in SWTDL output. When driving the input transducer of a SWTDL, the transformer produces a peak voltage of approximately 24 volts across the transducer. A typical oscillogram of the transformer output (driving a SWTDL input transducer) is shown in Figure 9a. The negative transient immediately following the pulse is due to inductive ringing in the transformer. The majority of the ringing caused by the transformer was eliminated by placing a transient suppression diode across the transformer output as shown in Figure 8 and the remnant ringing is that evident in Figure 9a. The frequency spectrum of the pulser is shown in Figure 9b. Measurements indicated that the spectral energy produced by the pulser at 70 MHz was approximately 8 dB lower than the energy at 40 MHz.

4. SWTDL MODULES

The 127-chip SWTDL's are placed in self-contained modules along with their pulser circuits, matching networks, and output amplifiers. This packaging technique allows for maximum RF shielding between devices and, in addition, provides a convenient means of varying the synthesizer configuration in terms of center frequency, SWTDL codes, etc., because changes can be made at the module level.

The SWTDL modules were fabricated from double-sided copper-clad PC board material. Each module is a rectangular shaped box with a partition running down the middle (Figures 10 and 11). The SWTDL's are mounted on the partition (Figure 10.) and gold leads connect the SWTDL transducer to feed-through terminals which connect the input and output signals to the pulser circuit



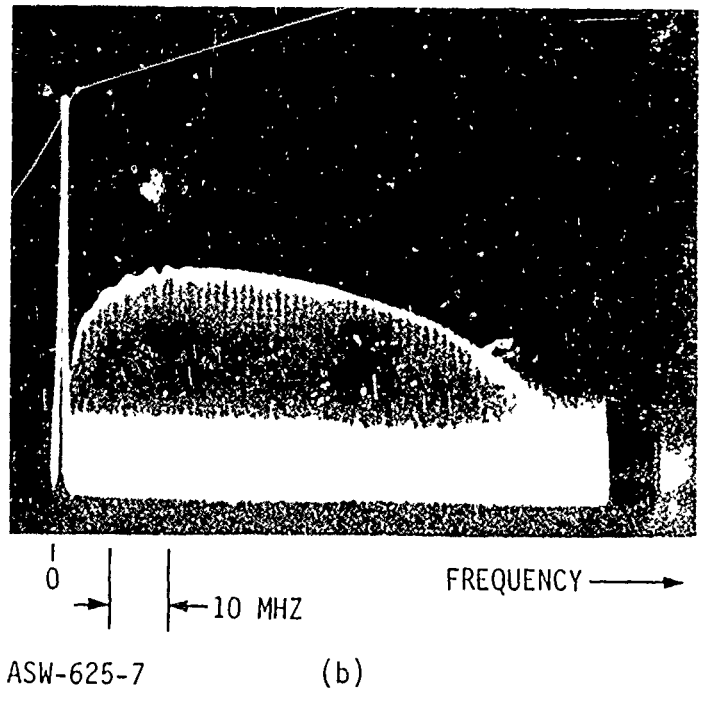


Figure 9. Pulser Output

and the output matching network. The pulser and matching network are mounted on the other side of the partition. The gold leads are fastened to the SWDL transducers with a silver epoxy cement which provides a good mechanical bond

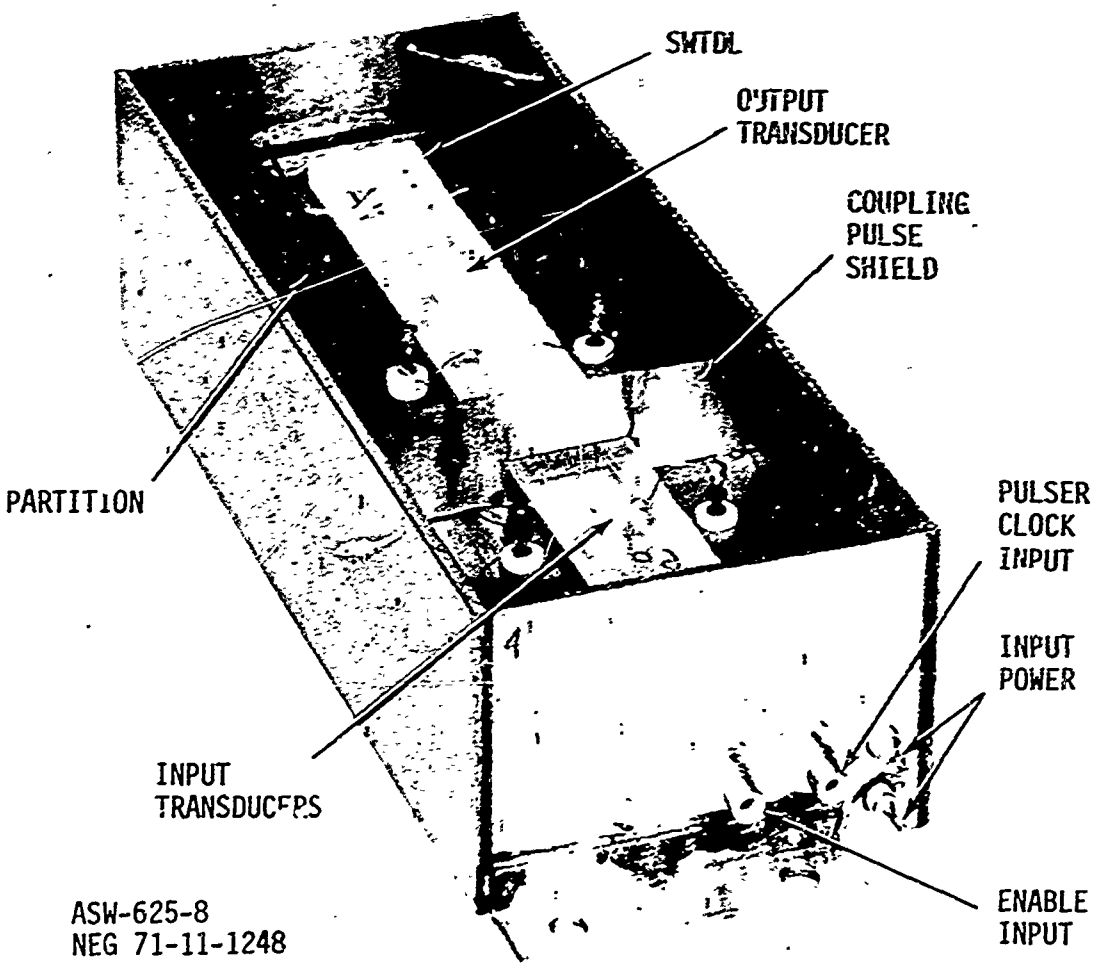


Figure 10. SWTDL Module, Top View

and a low RF resistance path. A top cover (not shown) protects the SWTDL surface from damage and at the same time allows the SWTDL to be electromagnetically shielded on all sides. A coupling pulse shield separates the input transducer from the output transducer in order to minimize the amount of energy coupled directly from the input transducer terminals to the output transducer terminals.

Figure 11 shows the position of the pulser circuit, output matching network, and output amplifier. The pulser circuit is mounted on a small PC board that is fastened to the center partition. A shield completely encloses the pulser circuit in order to eliminate coupling pulse radiation to the output matching network. The pulser clock and pulser enable signals and input power are fed into the module through subminiature connectors and capacitive feed-throughs.

The output matching network transformer is mounted on a small PC board which is in turn mounted to the output transducer feed-throughs. A short coaxial cable feeds the output signal from the tap on the transformer to the input of the SWTDL module amplifier. The SWTDL module amplifier (Avantek, Type UA-151) provides 20 dB of gain to the output signal and delivers it to a subminiature RF connector on the far end (in Figure 11) of the SWTDL module.

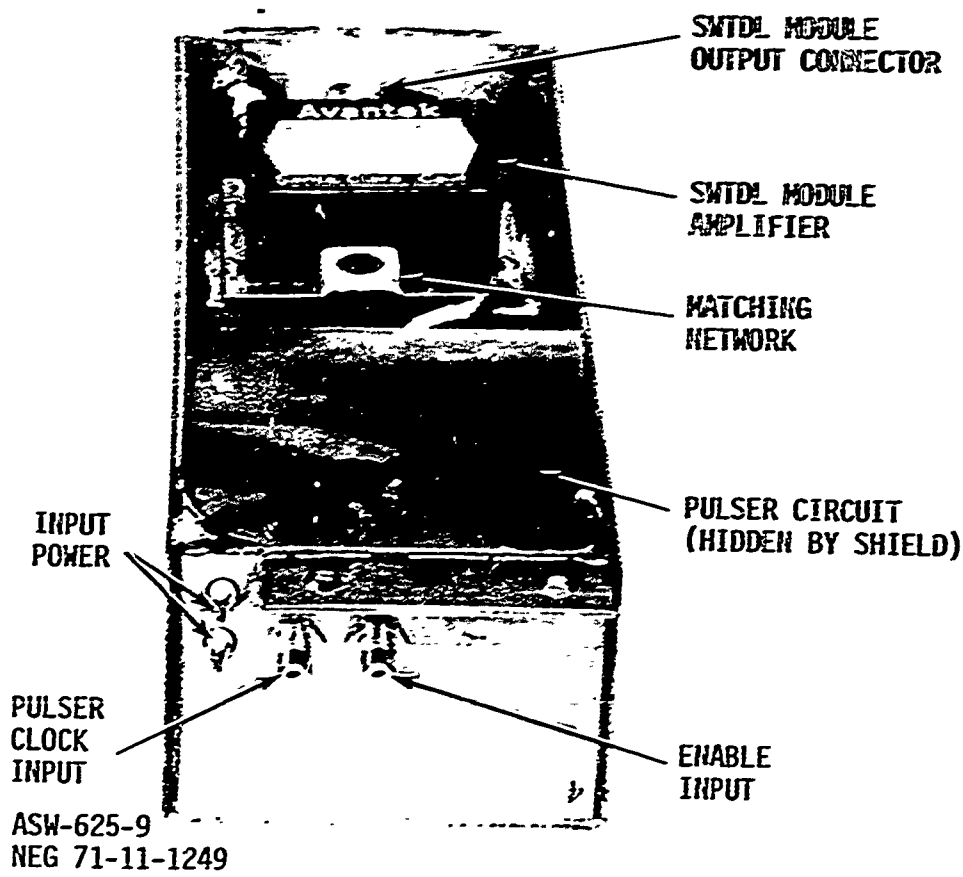


Figure 11. SWTDL Module, Bottom View

The physical design of each SWTDL module is identical. When mounted on the synthesizer chassis, the bottom of each module is completely enclosed (and thus shielded). All that is required for SWTDL module operation are appropriate TTL compatible pulser clock and enable signals and input power (+12 Vdc and +5 Vdc). The output of each module consists of the impulse response (of the particular SWTDL mounted in the module) at a level of approximately -55 dBm into 50 ohms. The signal-to-noise ratio of all eight modules built measured +18 dB in a 20-MHz bandwidth when the modules were pulsed at a 78.7401 kHz (continuous output signal) rate.

5. LOGIC DESIGN

With the exception of the Schottky clamped TTL logic used in the SWTDL module pulser circuits, all of the logic used in the synthesizer is composed of conventional dual in-line packaged TTL. The majority of the logic is contained on two printed circuit cards and includes the frequency-divider circuit (divide-by-127 and divide-by-60K) and the frequency-hop sequence generator.

a. Divide-by-127 Circuit

The 10-MHz system clock is divided by 127 to obtain a 78.7401 kHz clock for Mode I operation, using a slightly modified binary ripple counter. A block diagram of the counter is shown in Figure 12. The most important design requirement on the counter is that it produces a pulser clock signal with a period of precisely 12.7 microseconds in order to maintain synthesizer coherency. If an ordinary ripple counter were used to divide the 10-MHz clock, variations in the ripple time with temperature and power supply would cause variations in the time position of the pulser clock relative to the 10-MHz system clock. In order to avoid these variations, the counter of Figure 12 operates by counting up to 126, resetting to zero, counting up to 126, etc. An AND gate looks at the six most significant bits in the counter and AND's these six bits with the 10-MHz clock. When the 126th clock pulse occurs, it ripples through the counter. Before the 126th clock pulse has rippled completely through the counter, the 10-MHz clock falls low and the AND circuit is disabled. After the 126th clock pulse has completely rippled through the counter, the six most significant bits fed to the AND gate are true so that the following (127th) clock pulse enables the AND gate and produces an output (pulser clock) pulse. Thus, the pulser clock occurs on every 127th system clock pulse but is completely independent of any ripple time variations in the counter. As a result, the time position of the pulser clock signal is essentially determined by the stability of the system clock.

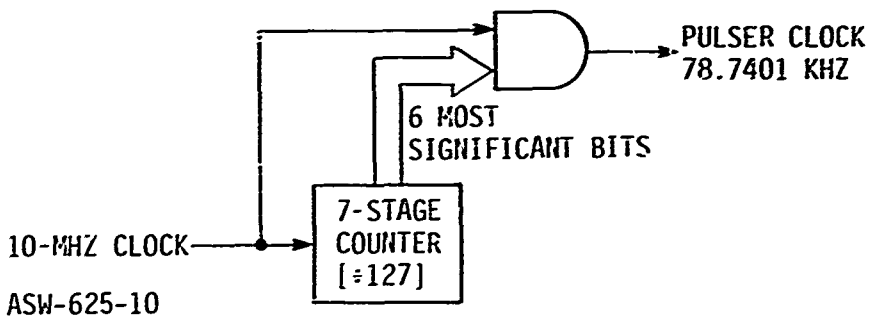


Figure 12. Divide-by-127 Circuit

b. Divide-by-60,000 Circuit

The divide-by-60,000 circuit is used to divide the 10-MHz clock down to 166.66 Hz for Mode II operation and, in general, uses the same operating principle as does the divide-by-127 circuit. The divide-by-60,000 circuit uses a 16-stage ripple counter that counts up to 59,999, resets to zero, counts up to 59,999, resets to zero, etc. The reset pulse (and pulser clock output) of the counter is determined solely by the time of occurrence of each 60,000th system

clock pulse and hence, the Mode II pulser clock is not affected by ripple time variations in the counter.

c. PN Sequence Generator

The PN sequence used to determine the frequency-hopping pattern is developed by a six-stage feedback shift register. The shift register is clocked by the pulser clock output of the frequency divider circuit and produces a maximal length binary sequence 63 chips in length. The feedback tap equation for the generator is $Am = Am_{-1} \oplus Am_{-6}$, (i.e., the first and sixth stages are used as the feedback terms). The generator employs zero suppression to eliminate the possibility of an all-zero state condition in the shift register.

d. Frequency Select Logic

The frequency select logic interprets the state of the PN sequence generator and generates four signals that serve as the pulser enable signals for the four SWTDL modules. These signals are formed by NORing the E, $\overline{E}$, F and $\overline{F}$ outputs of the PN sequence generator as shown in Figure 13. Using this scheme, only one pulser enable line can be logically true at any one time and hence only one of the four pulsers can be enabled at any one time.

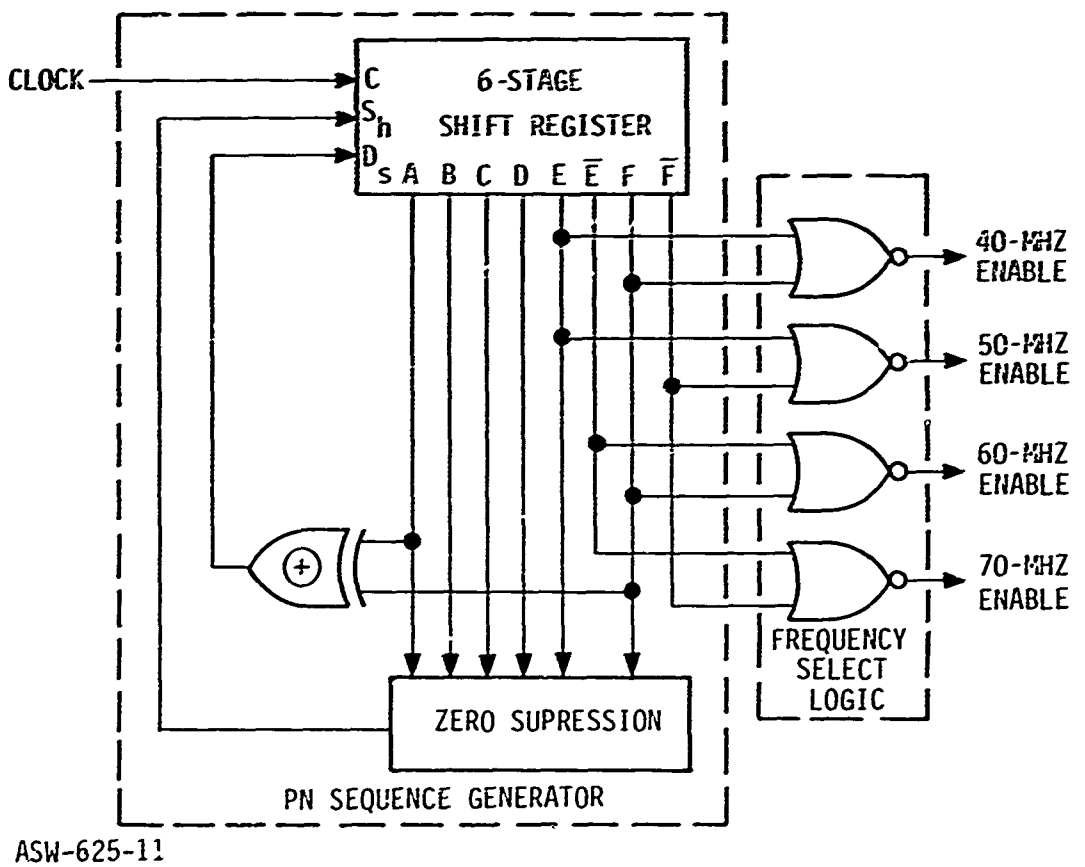


Figure 13. PN Sequence Generator and Frequency Select Logic

6. RF GATING

The output of each SWTDL module is fed through an RF gate prior to combining of the four signals in order to preserve the signal-to-noise ratio of the resultant signal at the synthesizer output. Since each SWTDL module contains its own output amplifier, the output of each module consists of a 12.7-microsecond SWTDL impulse response when the SWTDL is pulsed, plus a random noise component generated by the SWTDL output amplifier. This noise signal is present whether the SWTDL is pulsed or not. If the four SWTDL outputs were combined without RF gating, the resultant signal would consist of the SWTDL output signal power P_s, plus the output noise power of its output amplifier P_n, plus the output noise power of the three other SWTDL amplifiers. Since the output amplifiers and their effective noise bandwidths are identical, and since their noise powers are uncorrelated, the total output noise power would be $4P_n$ and the resultant synthesizer output signal-to-noise ratio would be $P_s/4P_n$. However, by gating only the signal generated by a pulsed SWTDL module to the synthesizer output, the resultant signal-to-noise ratio is P_s/P_n which is a 6 dB improvement over the ungated case.

By increasing the synthesizer output signal-to-noise ratio, the degree of coherency achievable between a pair of otherwise (perfectly) matched synthesizers is improved, since noise manifests itself as a random phase jitter on the synthesizer outputs. In a practical situation, where the synthesizers would form part of a communication system, the signal-to-noise ratio at the synthesizer outputs would have a direct bearing on the performance of the system.

a. Gate Electronics

The RF switches used for gating and the electronics required to drive them are contained in a switch module. A block diagram of one of the switch circuits is shown in Figure 14 and an interior view of the switch module is shown in Figure 15. The switch, a Relcom Type S-7C, is driven by a bipolar constant current source. The constant current source supplies +20 milliamperes when the switch is turned on and -20 ma when the switch is turned off. Normally, the switch is turned off. However, when the switch enable line is enabled by the frequency select logic, a 12.7-microsecond one-shot (contained in the switch module) is fired and this in turn causes the current supplied to the RF switch to change from -20 milliamperes (the off condition) to +20 milliamperes (the on-condition) for 12.7 microseconds. At the end of the 12.7-microsecond period, the one-shot times out and the current supplied to the RF switch reverts back to -20 milliamperes.

In order to prevent the current supplied to the RF switch from changing instantaneously (and thus causing a switching spike at the switch output), the bipolar constant current source output is integrated by capacitor C so that the current supplied to the switch changes linearly and at a controlled rate. (The current changes polarity in about 500 nanoseconds in the present design).

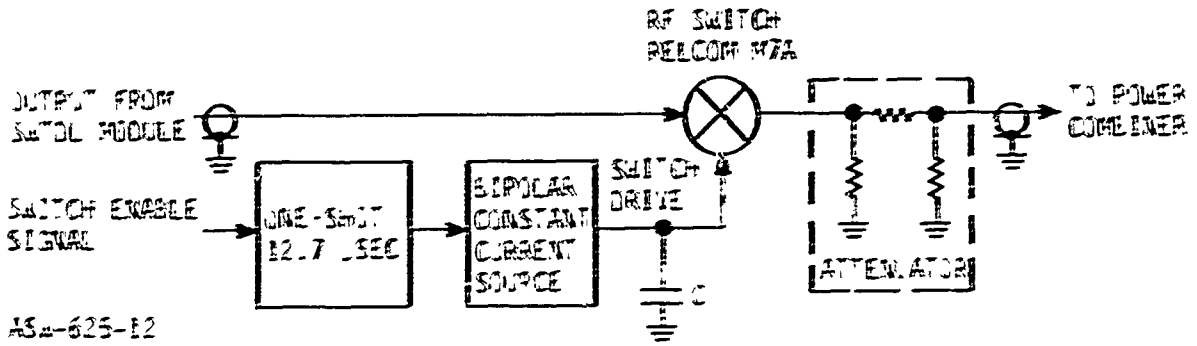


Figure 14. RF Switch Circuit

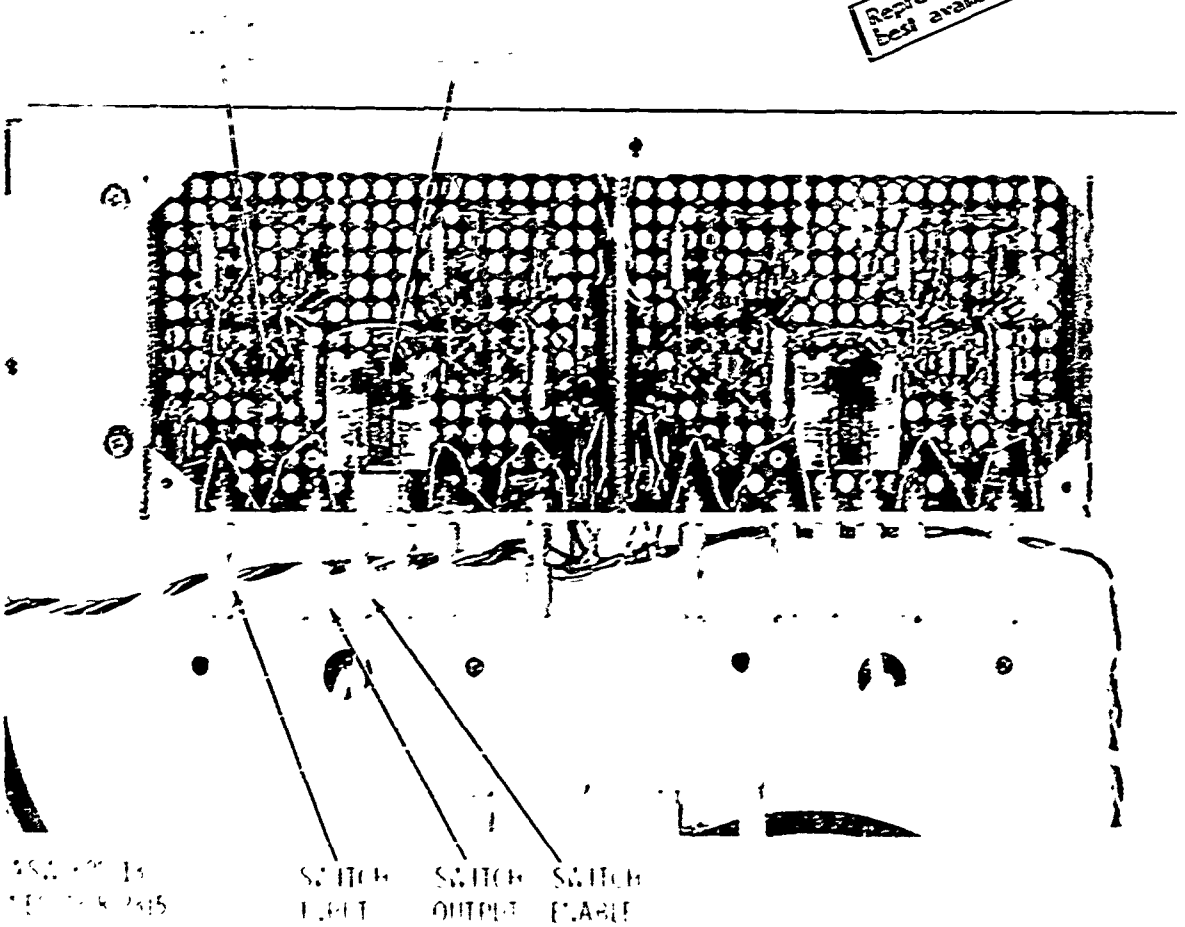


Figure 15. Switch Module

b. Switch Enable Signals

The switch enable signals for the RF switch circuits are generated in the frequency-hop sequence generator. These signals follow the same sequence as do the pulser enable signals, but are delayed in time approximately 4.9 microseconds. The 4.9-microsecond delay is necessary to account for the delay that occurs between pulsing a SWTDL and obtaining a SWTDL impulse response (a consequence of the physical separation between input and output transducers on the SWTDL substrates). Thus, when a particular SWTDL impulse response is just beginning, its corresponding RF switch has just turned on and remains on for the 12.7-microsecond duration of the impulse response.

The switch enable signals are generated as shown in Figure 16. Pulser clock triggers a 4.9-microsecond one-shot and its output is ANDed with the 40, 50, 60, and 70-MHz pulser enable signals. The one-shot is configured such that after it has timed out, it enables all four AND gates. The particular AND gate that is at that time also enabled by a pulser enable signal thus produces a switch enable signal.

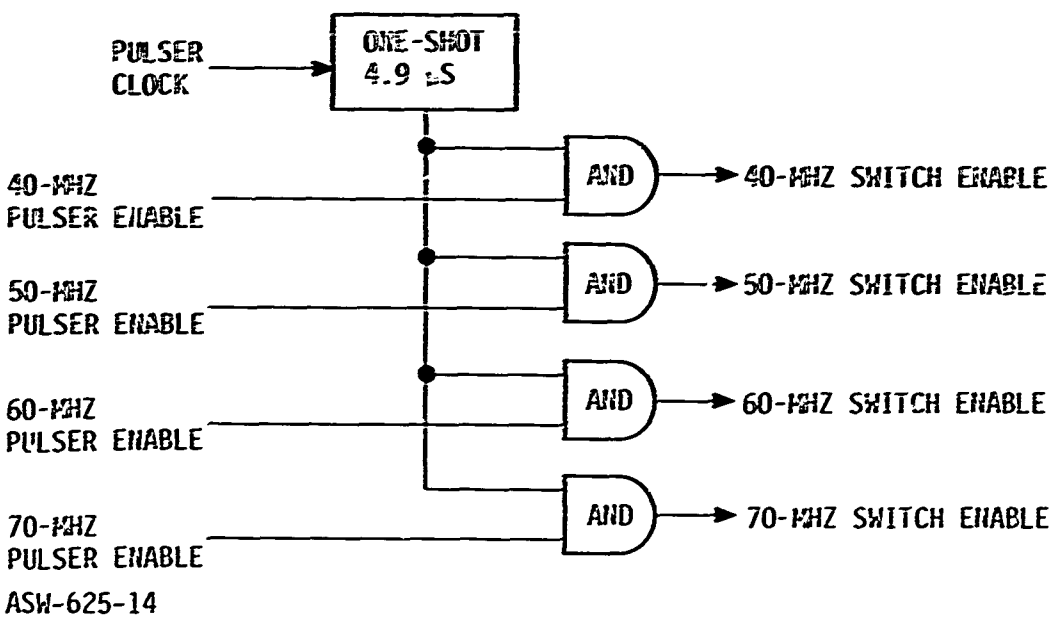


Figure 16. GATE Enable Generation

c. Output Attenuators

The output of each RF switch is fed through an attenuator before leaving the switch module. The purpose of the attenuators is to equalize the SWTDL outputs so that the average signal level of the synthesizer output is the same from frequency-hop to frequency-hop. The attenuators are resistive Pi pads designed for input and output

impedances of 50 ohms so that, in addition to equalizing the SWTDL module outputs, the attenuators provide a solid 50-ohm termination for the RF switch and power combiner.

7. SIGNAL SUMMATION

Summation of the SWTDL output signals is performed using a five-port reactive hybrid power combiner, (a Merrimac Research model PD-40-55). This device provides essentially lossless combining of the SWTDL outputs, while providing excellent phase and amplitude balance between signals. A reactive hybrid is used rather than a resistive summer in order to avoid the rather large insertion loss that would be suffered using a resistive summer.

8. OUTPUT GAIN

The output of the power combiner is fed to an amplifier module which provides 60 dB of gain. The amplifier module is composed of a cascade of two Avantek UA-151 amplifiers followed by an Avantek UA-152 amplifier. All three of these amplifiers are characterized by their wide bandwidth (20 to 250 MHz), flat amplitude response (±0.5 dB from 20 to 250 MHz), and linear phase response, (a measured 3-degree deviation from perfect phase linearity over the 30 to 80-MHz frequency range). The UA-152 amplifier has a relatively high 1 dB compression point (+10 dBm) and this allows it to provide a synthesizer output level of approximately -5 dBm into 50 ohms that is free from spurious products.

The UA-151 amplifiers are identical in gain, bandwidth, and amplitude flatness to the UA-152. The UA-151 has a somewhat better noise figure (3.5 dB), than the UA-152 and hence is used as the first two stages in the output amplifier chain. (Because of their excellent noise figure, UA-151's are also used as the SWTDL output amplifiers in the SWTDL modules).

9. SYNCHRONIZATION

a. Frequency-Hop Synchronization

Synchronization of the frequency-hop sequence generators in synthesizers No. 1 and No. 2 is performed by means of the synchronization circuitry shown in Figure 17. As mentioned previously, the frequency-hopping sequence is generated using a six-stage feedback shift register. In synthesizer No. 1, the six states of the shift register are continuously monitored by a sync recognition gate. The sync recognition gate recognizes the 6-bit sequence 101010. This sequence occurs only one time per 63-bit PN frame. When this point in the PN frame occurs and is recognized, the sync recognition gate sends a pulse to the data input of a D flip-flop. The flip-flop is clocked by pulser clock and transfers the logic level at its data input to its output on each clock pulse. Normally the data input is low and, therefore, the flip-flop output is low. When the 6-bit sync sequence is recognized however, the flip-flop data input goes high and, therefore, the D flip-flop output is clocked high and forms the PN sync pulse sent to synthesizer No. 2.

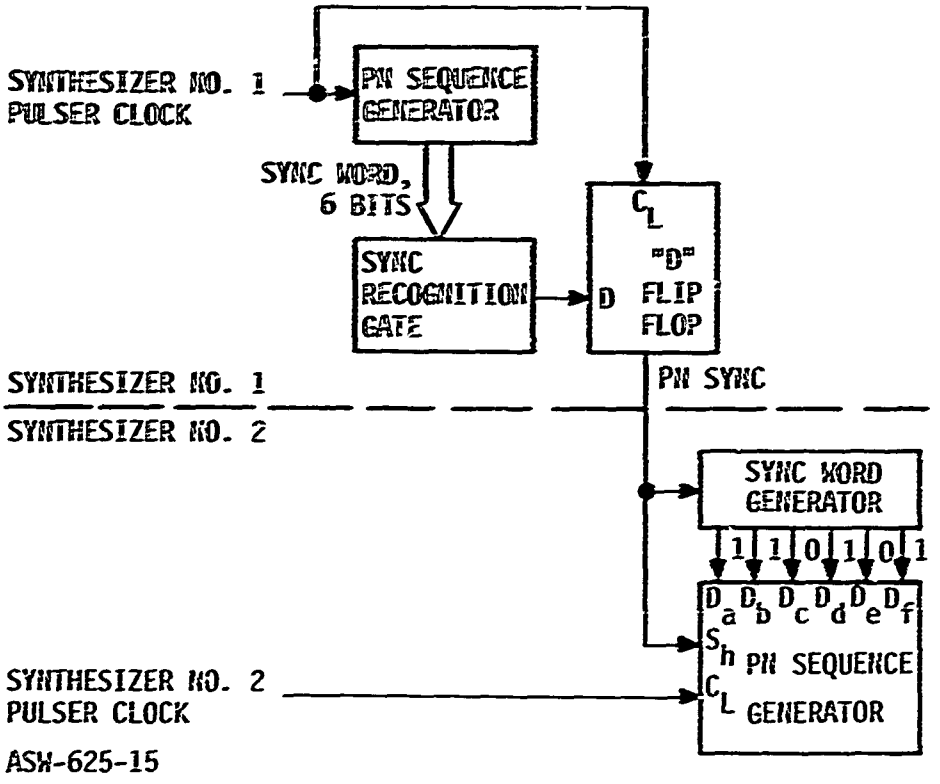


Figure 17. Frequency-Hop Synchronization

The PN sequence generator in synthesizer No. 2 is basically the same type of sequence generator as is used in synthesizer No. 1, but in addition, it has a sync word generator. The PN sequence generator in synthesizer No. 2 operates exactly the same way as does the PN sequence generator in synthesizer No. 1 except for when a PN sync pulse occurs. When the PN sync pulse occurs, a 6-bit sync word is parallel-transferred into the six stages of the shift register forming the synthesizer No. 2 PN sequence generator. This 6-bit word is generated by the sync word generator as a result of the occurrence of the PN sync pulse. The sync word generator maintains the 6-bit word until the next clock pulse occurs following the clock pulse that caused PN sync to be recognized in synthesizer No. 1. When this clock pulse occurs, the PN sequence generator in synthesizer No. 1 cycles to the next state in the PN sequence (specifically 110101) and the 6-bit word that is transferred into the synthesizer No. 2 PN sequence generator is 110101. At this point, both PN sequence generators contain the 6-bit word 110101 and are therefore synchronized. As succeeding clock pulses occur, both PN sequence generators produce the same sequence of bits as the feedback logic in both sequence generators is the same.

b. Pulser Clock Synchronization

A synchronization circuit is required to insure that the pulser clocks in synthesizers No. 1 and No. 2 occur at the same time. (Pulser clock sync assumes that the 10-MHz clocks in both synthesizers are synchronized. In addition, pulser clock sync is required before frequency-hop synchronization can occur).

Pulser clock sync is obtained by comparing the pulser clocks produced by synthesizers No. 1 and No. 2 in a pulse comparator circuit. The comparator circuit is located in synthesizer No. 2 and pulser clock from synthesizer No. 1 (pulser clock No. 1) is hard wired over to synthesizer No. 2. The comparator circuit produces an enable signal which is used to control the 10-MHz clock pulses fed to the frequency divider circuit in synthesizer No. 2. Under normal operating conditions, when the pulser clocks are synchronized, the comparator circuit continuously enables (10 MHz) clock pulses to the synthesizer No. 2 frequency divider circuit. When the pulser clocks are not synchronized however, the comparator circuit detects this condition and (by means of its enable signal) deletes the (10 MHz) clock pulses from the 10-MHz clock fed to the frequency-divider circuit in synthesizer No. 2. The comparator circuit makes the enable-disable decision on every occurrence of pulser clock No. 2, thereby deleting one (10 MHz) clock pulse at a time until pulser clocks No. 1 and No. 2 are synchronized.

In Mode I operation, pulser clock is derived by dividing the 10-MHz clock by 127, thereby producing a 78.7401 kHz pulser clock rate In the worst-case condition, the synthesizer No. 2 divide-by-127 circuit could be out of sync with the synthesizer No. 1 divide-by-127 circuit by 126 states. Since the pulser clock comparator circuit makes a decision once every pulser clock (i.e., every 12.7 microseconds), the worst-case sync time in Mode I is 126 times 12.7 microseconds or 1.6 milliseconds.

In Mode II operation, pulser clock is derived by dividing the (10 MHz) clock by 60,000, thereby producing a 166.66 Hz pulser clock rate. In the worst-case condition, the synthesizer No. 2 divide-by-60,000 circuit could be out of sync with the synthesizer No. 1 divide-by-60,000 circuit by 59,999 states. Since, in this case, the pulser clock comparator circuit makes a decision once every 6 milliseconds, the worst-case sync time is 59,999 x 6 milliseconds or approximately 6 minutes. This synchronization time would be quite objectionable if the synthesizers were to be used in a data transmission system. However, for phase coherency testing, the 6-minute maximum sync time did not prove to be particularly bothersome. For this reason no attempt was made to reduce the Mode II pulser clock sync time. It should be realized however, that through a somewhat more complexly implemented synchronization circuit the worst-case Mode II sync time could be reduced to approximately 6 milliseconds.

c. VCXO Sync

The phase coherency between synthesizers is basically determined by the phase coherency between the 10-MHz clock in synthesizer No. 1 and the 10-MHz clock in synthesizer No. 2. The 10-MHz clock in synthesizer No. 1 is derived from an ovenized crystal oscillator with a short term stability of ±1 part in 10^{10} per minute. The 10-MHz clock in synthesizer No. 2 is derived from a 10-MHz VCXO which is phase-locked to the 10-MHz clock in synthesizer No. 1.

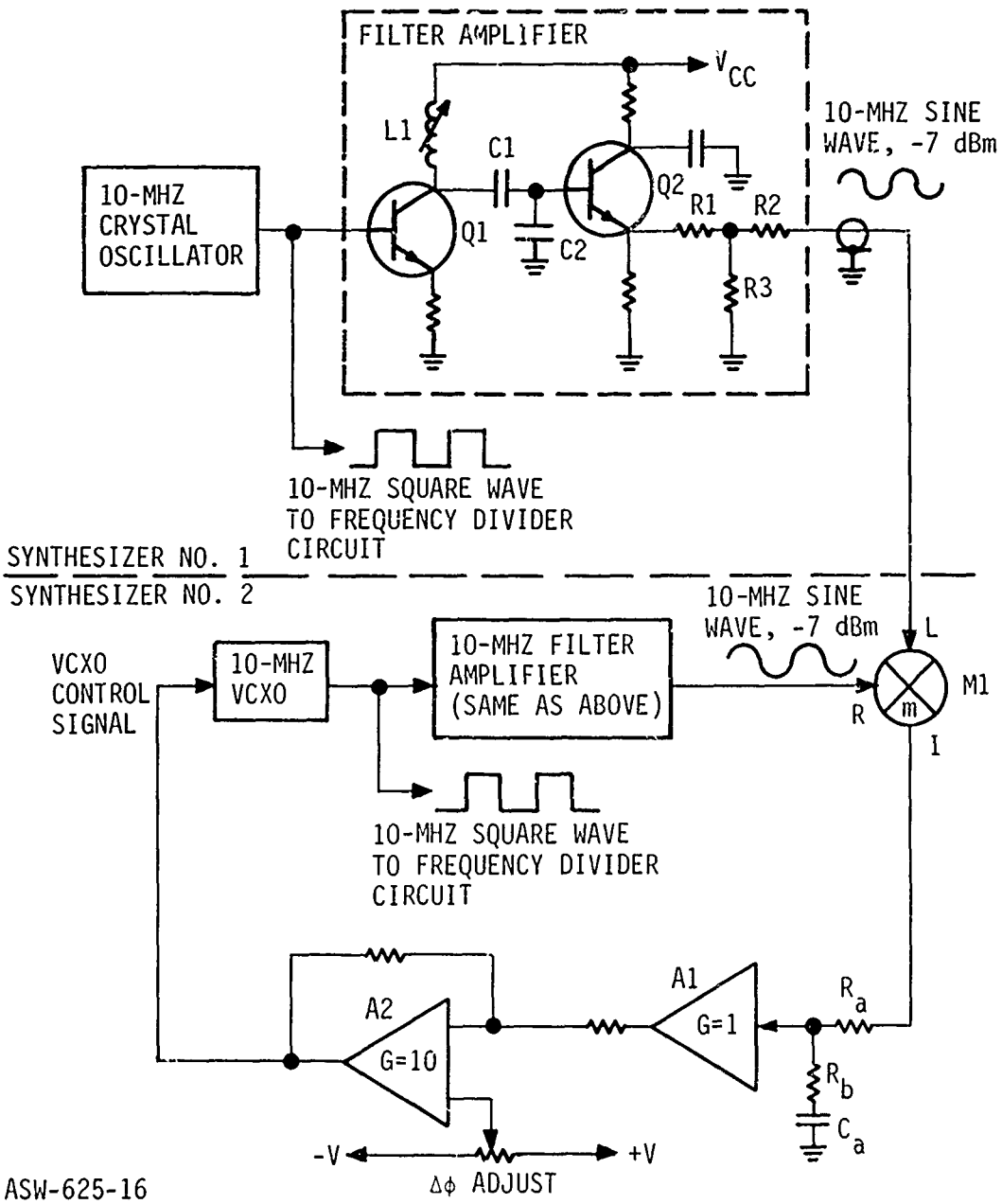


Figure 18. VCXO Sync Circuit

A block diagram of the VCXO sync circuitry is shown in Figure 18. The 10-MHz square wave produced by the 10-MHz crystal oscillator in synthesizer No. 1 is fed to a filter amplifier comprised of Q_1 and Q_2. Bias circuitry is omitted in the schematic for simplicity. The L_1, C_1, C_2 tank circuit is tuned to the 10-MHz funadmental of the square wave and produces a 10-MHz sine wave which is buffered by emitter follower Q2. The 10-MHz sine wave is fed through a resistive pad with a 50-ohm output impedance and then to synthesizer No. 2 via a coaxial cable.

The 10-MHz reference sine wave from synthesizer No. 1 is fed to the "L" port of a Relcom Type M1 double-balanced mixer located in synthesizer No. 2. The 10-MHz squre wave from the synthesizer No. 2 VCXO is filtered, amplified, and the resultant 10-MHz sine wave is fed to the "R" port of the double balanced mixer. The mixer functions as a phase detector and produces an error signal at its "I" port proportional to the cosine of the phase difference between the "L" and "R" port 10-MHz sine waves.

The error signal is fed to a loop filter comprised of lag-lead network R_a, R_b, C_a and amplifiers A_1 and A_2. Amplifier A_1 provides unity gain and a very high input impedance to prevent loading of the lag-lead network. Amplifier A_2 provides a voltage gain of 10 and also a dc offset adjust for the error signal. The output of A_2 is fed to the VCXO as its control signal. This circuit is a second-order phase lock loop with a loop bandwidth of 100 radians/second and damping factor of 0.5. The ϕ adjust control allows the relative phase of the synthesizer No. 1 and No. 2 10-MHz clocks to be adjusted so as to maximize the phase coherency between synthesizers.

10. MECHANICAL LAYOUT

The mechanical layout of the synthesizers is shown in Figures 19 through 26. Both synthesizers (Figure 19) are mounted in separate chassis measuring 16-5/8 inches wide by 13-1/4 inches deep by 5-1/4 inches high. The front panels of both synthesizers are identical and contain the system power switch, oscillator oven power switch, mode switch, and output connector (Figure 20). The oven power switch allows the 10-MHz oscillator primary power to be turned on while the rest of the system is off to enable the oscillator to stabilize.

The rear panel of synthesizer No. 1 (Figure 21) contains input power terminals (+5 vdc, +12 vdc, -12 vdc and +28 vdc) and, in addition, contains output connectors for the 10-MHz clock reference, pulser clock and PN sync pulse synchronization signals fed to synthesizer No. 2. An additional connector provides a Mode II timing pulse signal used in phase coherency measurements. (This is discussed later in Section V, Testing).

The rear panel of synthesizer No. 2 is shown in Figure 22. It contains input power terminals and connectors for the 10-MHz reference, pulser clock,

and PN sync pulse synchronization signals generated by synthesizer No. 1. A connector which provides a replica of the 10-MHz VCXO square wave output is also available as a convenience for testing purposes.

Each synthesizer chassis is separated in the middle by a chassis plate. A top view of synthesizer No. 1 (Figure 23) shows the placement of 10-MHz crystal oscillator, 10-MHz filter amplifier, the four SWTDL modules, and the frequency-divider and hopping sequence generator digital logic cards. The top view layout of synthesizer No. 2 is essentially the same and is shown in Figure 24.

The bottom view of synthesizer No. 1 (synthesizer No. 2 is identical) is shown in Figure 25. As can be seen, the RF switch module, power combiner, and output amplifier do not occupy very much space. It is evident from Figures 23 through 25 that the synthesizers size could have been made significantly smaller if the need had arisen.

Figure 26 shows a top view of synthesizer No. 2 with the frequency-divider and hopping sequence generator logic cards tilted up for access. The logic cards (three in each synthesizer), are hinged on one end so that they may be tilted upright to be worked on. Normally the cards lie parallel to the chassis plate. Three cards were provided for each synthesizer but only two each were used, one for the frequency divider circuit and one for the hopping sequence generator. The third card was provided as a spare for future system expansion (i.e., for modulation circuits and so forth).

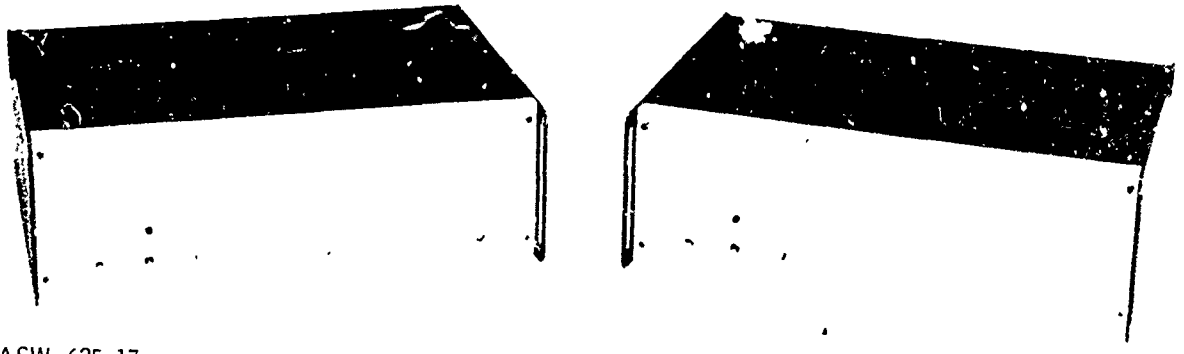


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Figure 19. Synthesizers No. 1 and No. 2

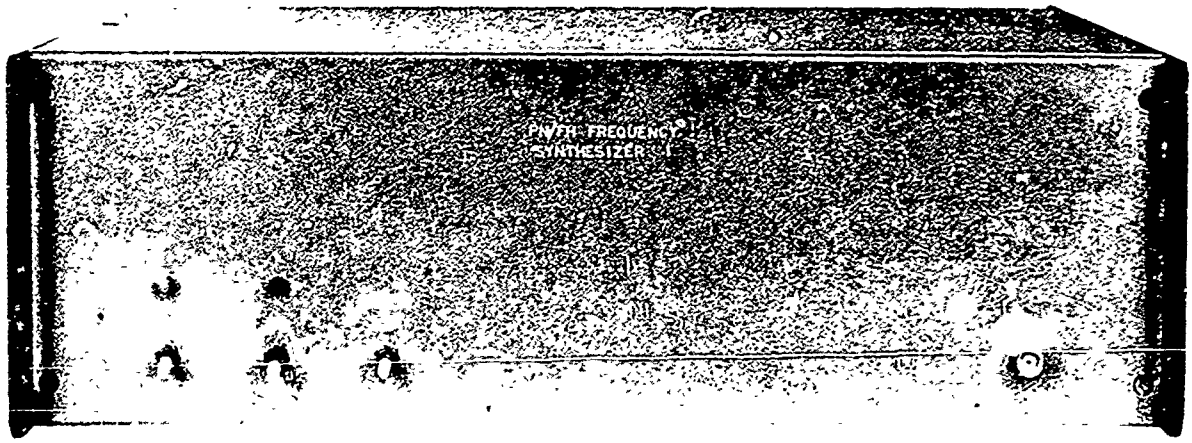

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Figure 20. Synthesizer Front Panel

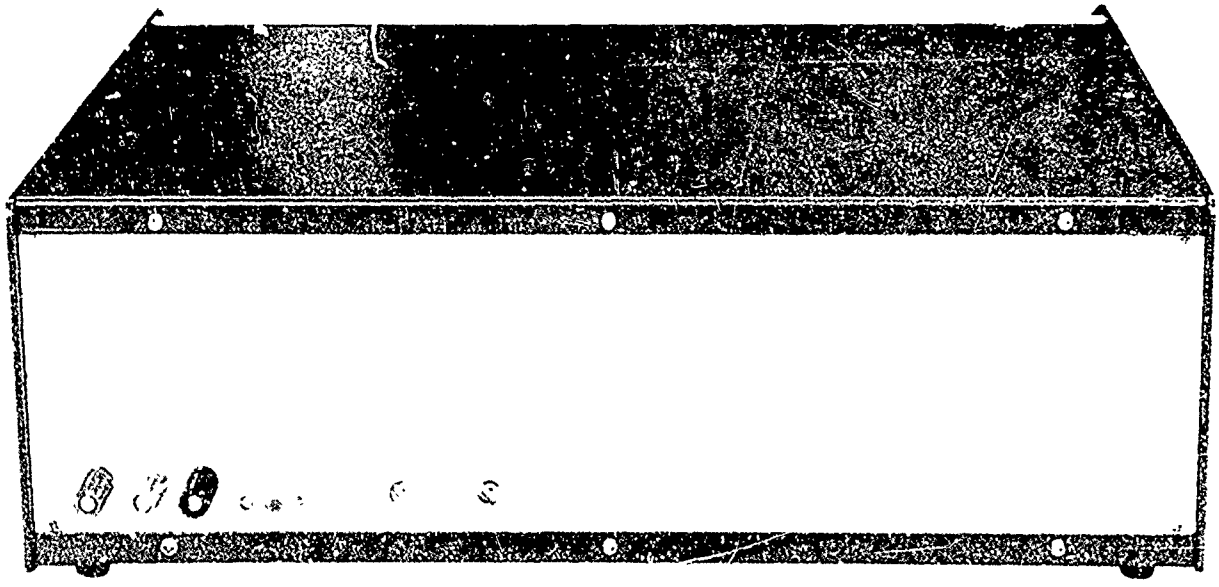

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Figure 21. Rear Panel, Synthesizer No. 1

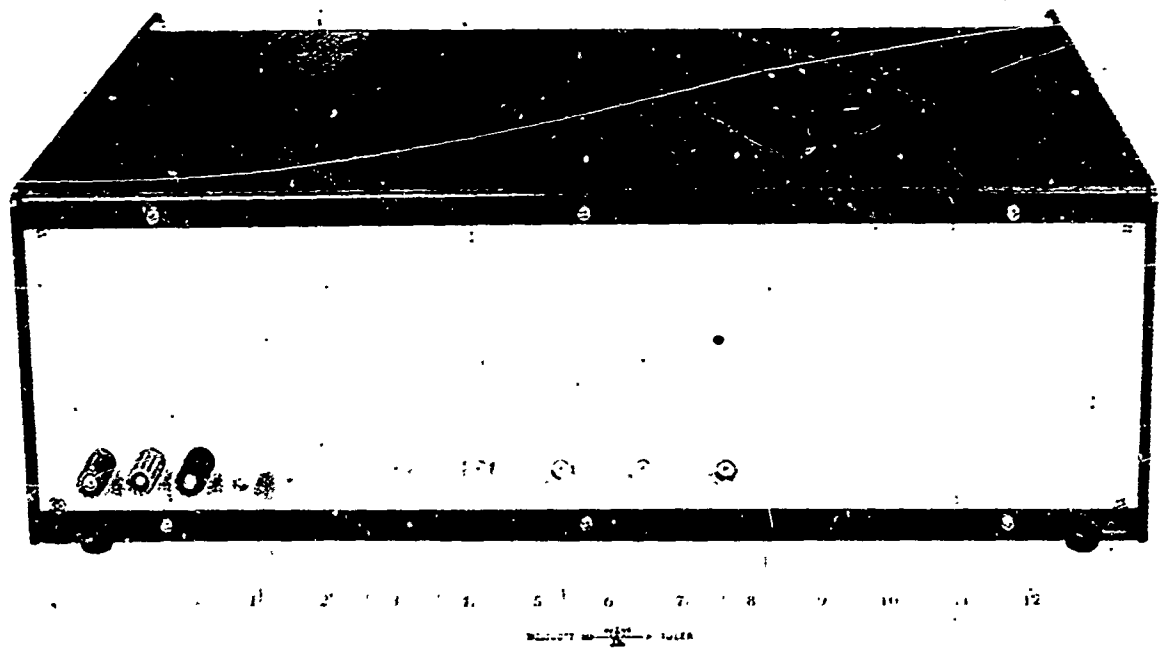

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Figure 22. Rear Panel, Synthesizer No. 2

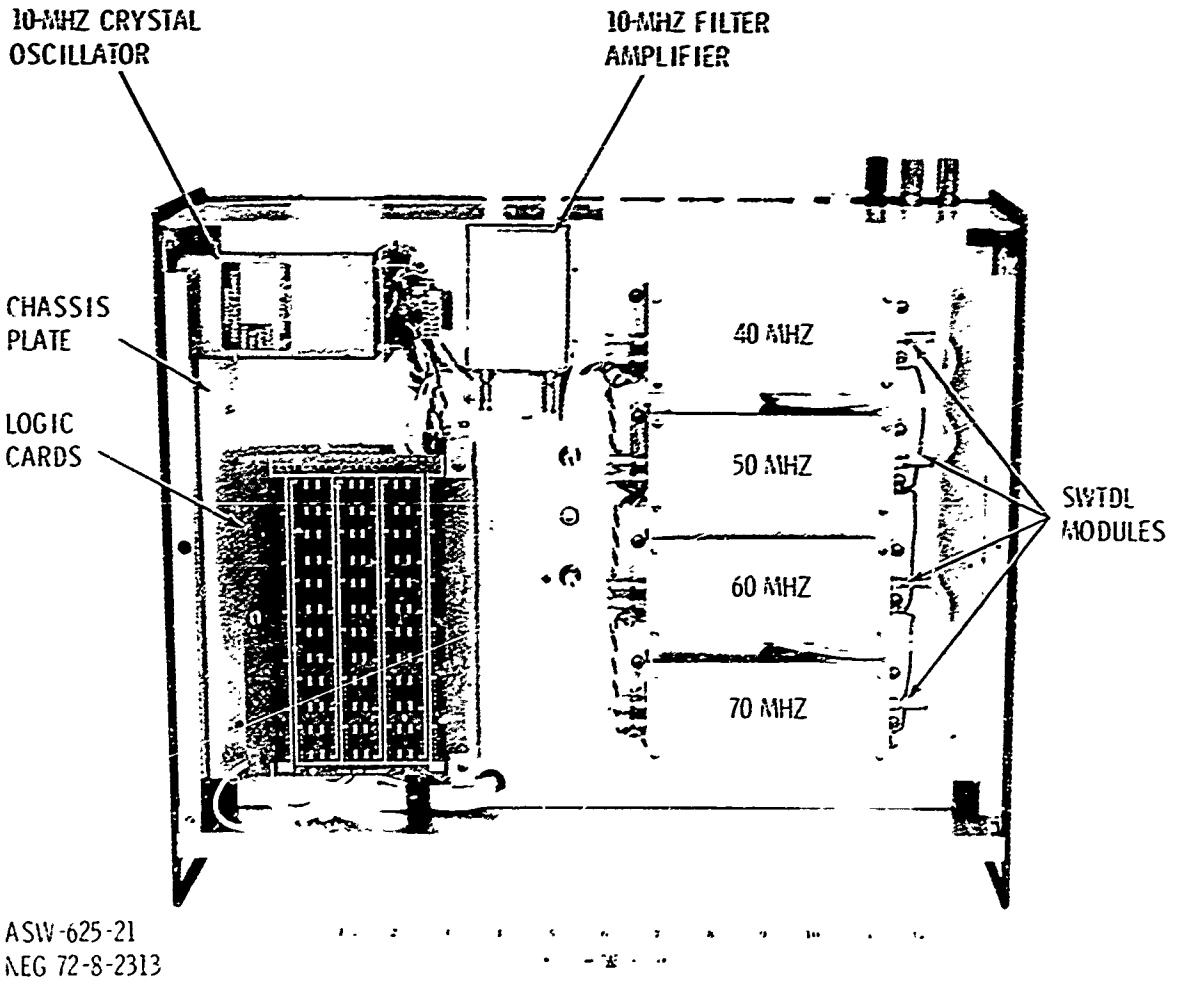

Figure 23. Top View, Synthesizer No. 1

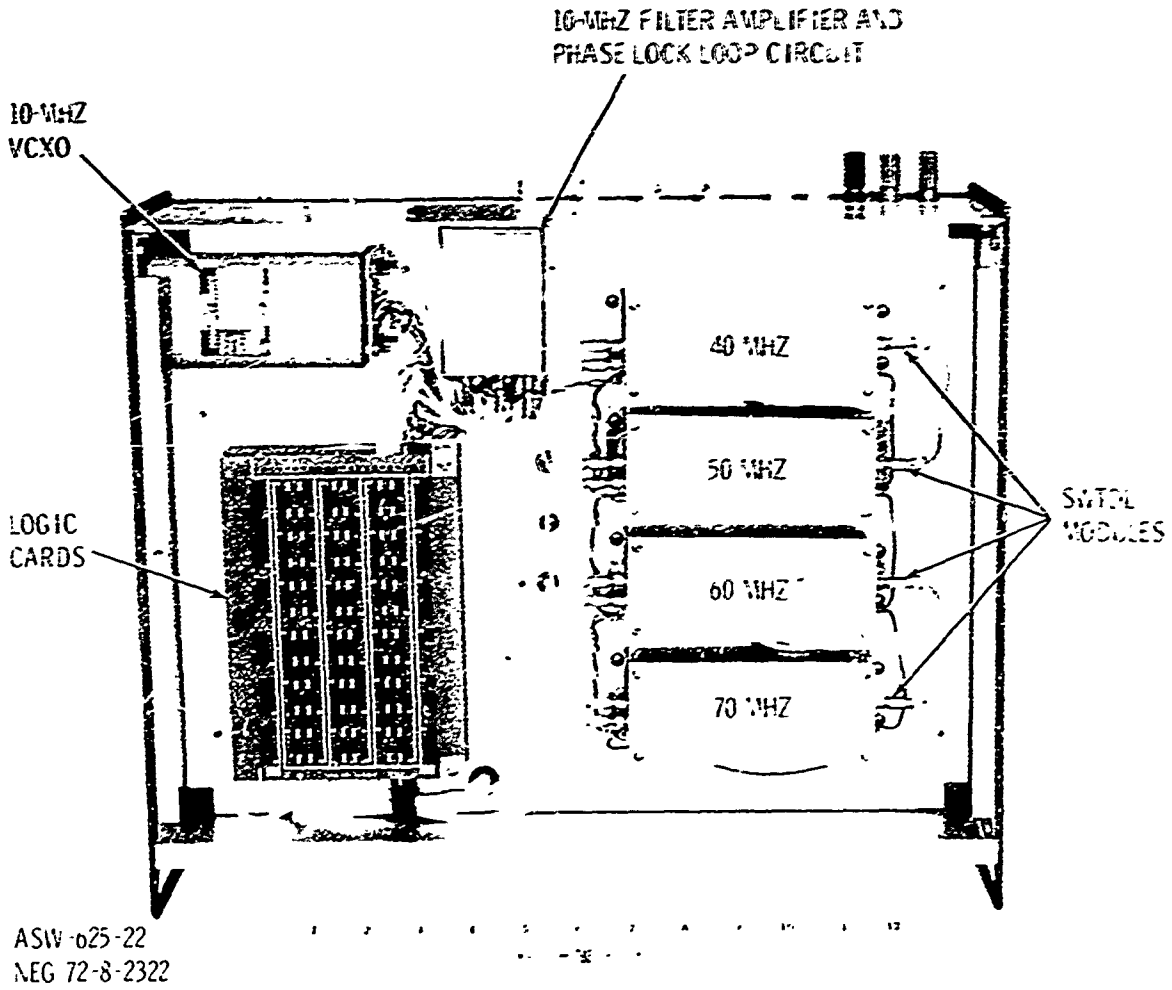

Figure 24. Top View, Synthesizer No. 2

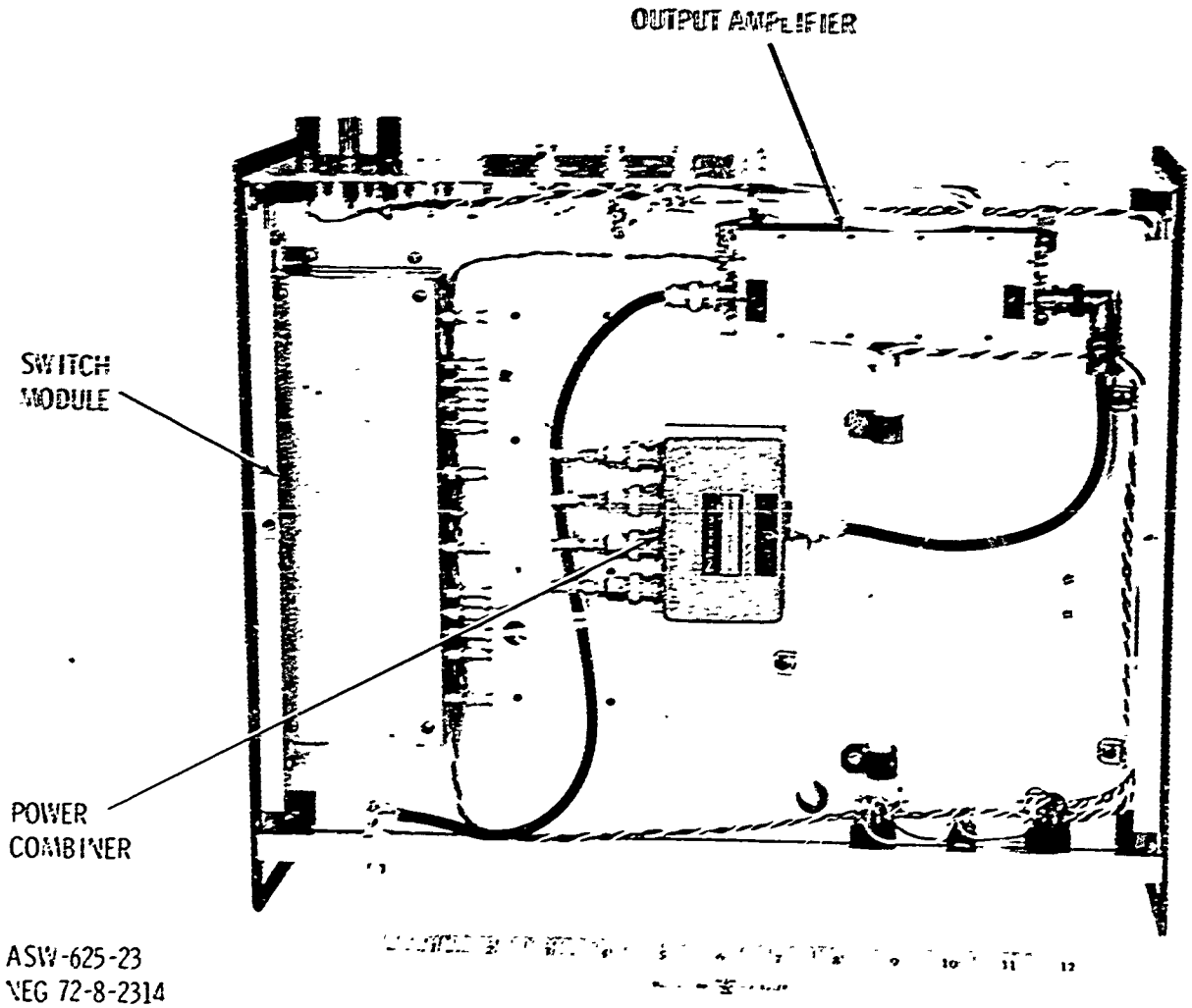

Figure 25. Synthesizer Bottom View

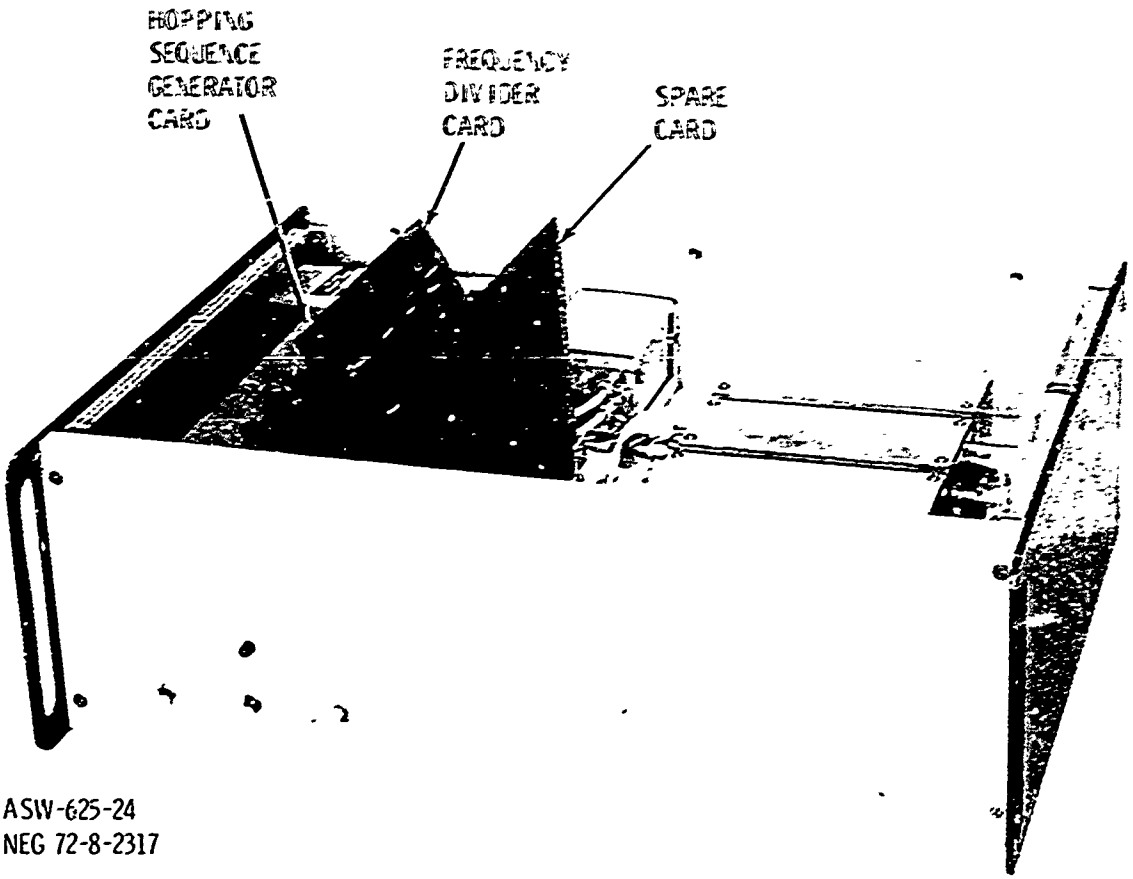

Figure 26. PC Card Access

SECTION V

TESTING

The primary goal of system testing of the two synthesizers was the determination of the degree of phase coherency attainable between synthesizers when operating in Mode I and Mode II conditions. The measurements of phase coherency between synthesizers required the fabrication of a coherency test set and the following paragraphs describe the theory of operation of the test set and the procedures used during coherency testing.

1. THEORY OF PHASE COHERENCY TESTING

When the two synthesizers are synchronized, the zero crossing of their output waveforms should (ideally) coincide at all times if perfect phase coherency is achieved. The degree to which the zero crossings do not coincide is, therefore, a measure of the incoherency between synthesizers. The requirements on the phase coherency test set were then the determination of the RMS value of the variation in zero crossings as the synthesizers hopped about in frequency.

The basic method chosen for measuring phase coherency between synthesizers was that of multiplying the synthesizer outputs by each other in a double-balanced mixer. As the result of this operation, a signal evolves that is proportional to the phase difference between synthesizers. (A double-balanced mixer, when used as a product detector, produces an output proportional to the cosine of the instantaneous phase difference between input signals.)

2. PHASE COHERENCY TEST SETUP

A block diagram of the phase coherency test setup is shown in Figure 27. The 10-MHz oscillator used as clock in synthesizer No. 1 and the 10-MHz VCXO used as clock in synthesizer No. 2 are shown separate from their respective synthesizers in order to simplify the test setup description. It is assumed that the 10-MHz clocks, pulser clocks, and frequency-hopping sequences of the two synthesizers are synchronized via the synchronization circuits previously described.

The phase coherency test set has two channels: A and B. The output of synthesizer No. 1 is fed to channel A, while the output of synthesizer No. 2 is fed to channel B. Ideally, the output of each synchesizer is a constant envelope biphase modulated signal. In practice, the signal will have amplitude modulations due to band limiting of the surface wave device outputs (they are acoustically bandlimited to 10 MHz by the input and output tranducers). In addition, slight variations between surface wave device output amplitudes exists and this cannot, in practice, be perfectly compensated by the equalizing attenuators in the switch module. In order to eliminate these amplitude variations from the phase coherency measurements, the output of each synthesizer is, therefore, fed through a wideband limiter in the test set in order to strip off the amplitude modulations.

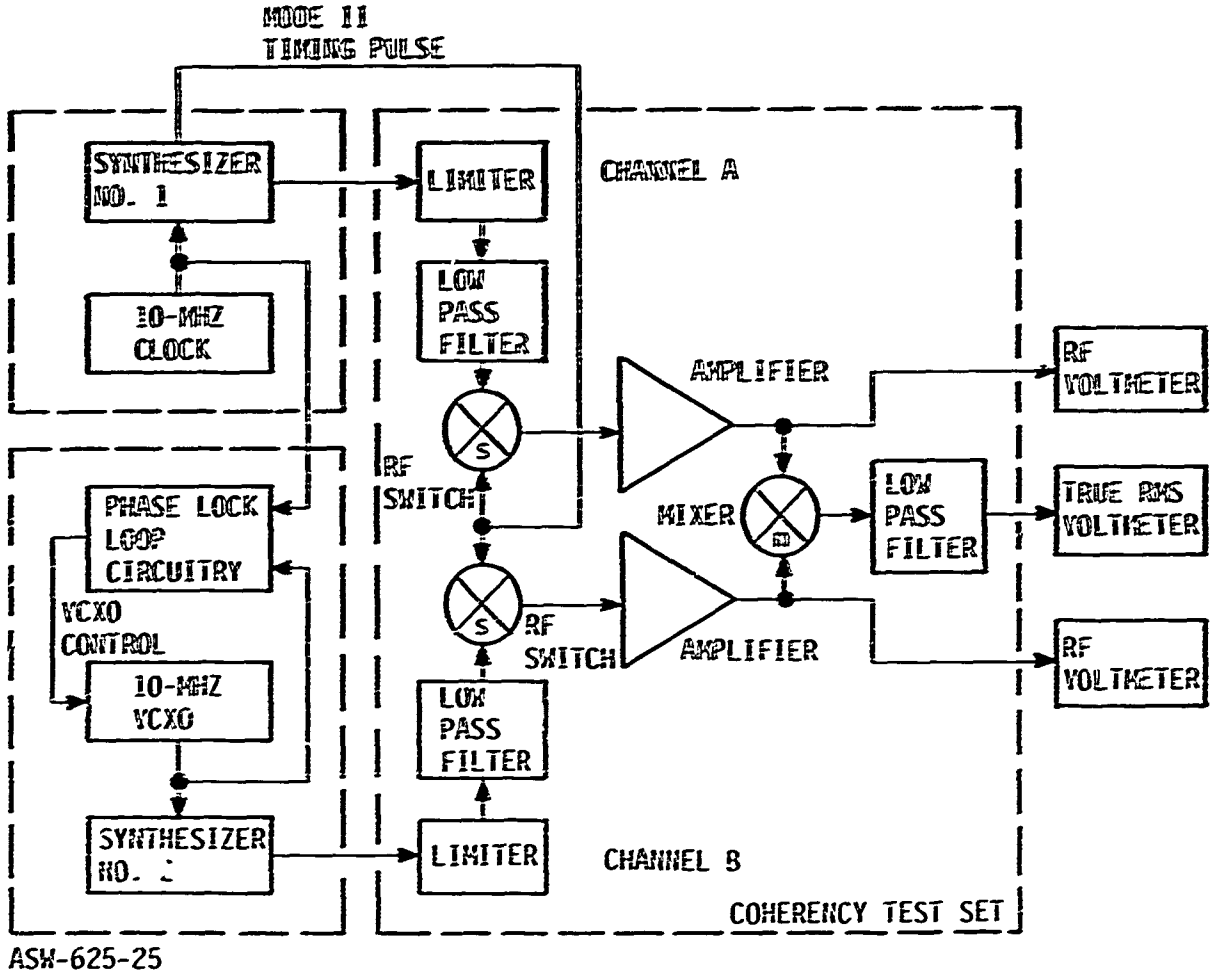

Figure 27. Phase Coherency Test Setup

Each limiter output consists of the fundamental component of its input signal plus odd harmonics of the input signal. Therefore, for an input signal centered at 40 MHz, the limiter produces an output at 40 MHz, 120 MHz, etc. In order to eliminate the effect of the odd harmonics, the limiter outputs are lowpass-filtered. The lowpass filters cut off at approximately 75 MHz in order to pass the fundamental component of the 70-MHz SWTDL outputs. The outputs of the lowpass filters are fed through RF switches (necessary for Mode II coherency testing and described later), are amplified, and are fed to a double-balanced mixer used as a phase detector. The mixer multiplies the two signals and produces an output composed of a double-frequency component and a second component which is a function of the instantaneous phase difference between synthesizer outputs. The mixer output is lowpass-filtered to remove the double-frequency component and the result is fed to a true RMS voltmeter that provides data to determine the RMS value of the synthesizer phase difference. RF voltmeters monitor the signal levels fed to the balanced mixer in order to eliminate the effect of mixer input signal variations from the phase coherency measurement. A detailed analysis of the mathematics involved in the phase measurement process is given in Appendix A.

In Mode II, the synthesizer outputs occur for periods of 12.7 microseconds at 6 milliseconds intervals. During the remaining time, the mixer receives a random phase signal from the limiters which could cause errors in the coherency measurement. In order to eliminate these errors, the limiter outputs are suppressed when the synthesizer outputs are zero by means of the RF switches previously described. The RF switches are turned on by a Mode II timing pulse generated by synthesizer No. 1. The pulse occurs just prior to a burst of RF from the synthesizers and turns the RF switches on for 12.7 microseconds every 6 milliseconds. In Mode I operation, the RF switches remain on continuously, since in Mode I the synthesizer outputs are continuous. A photograph of the phase coherency test set is shown in Figure 28.

3. TEST PROCEDURES

As described mathematically in Appendix A, the phase coherency test procedures involve the measurement of the test set output signals when the synthesizer No. 1 signal is compared with itself in the test set and when the synthesizer No. 1 output is compared with the output of synthesizer No. 2. The measurement of synthesizer No. 1 against itself is required in order to determine a (perfect coherency) reference signal from the test set. This is

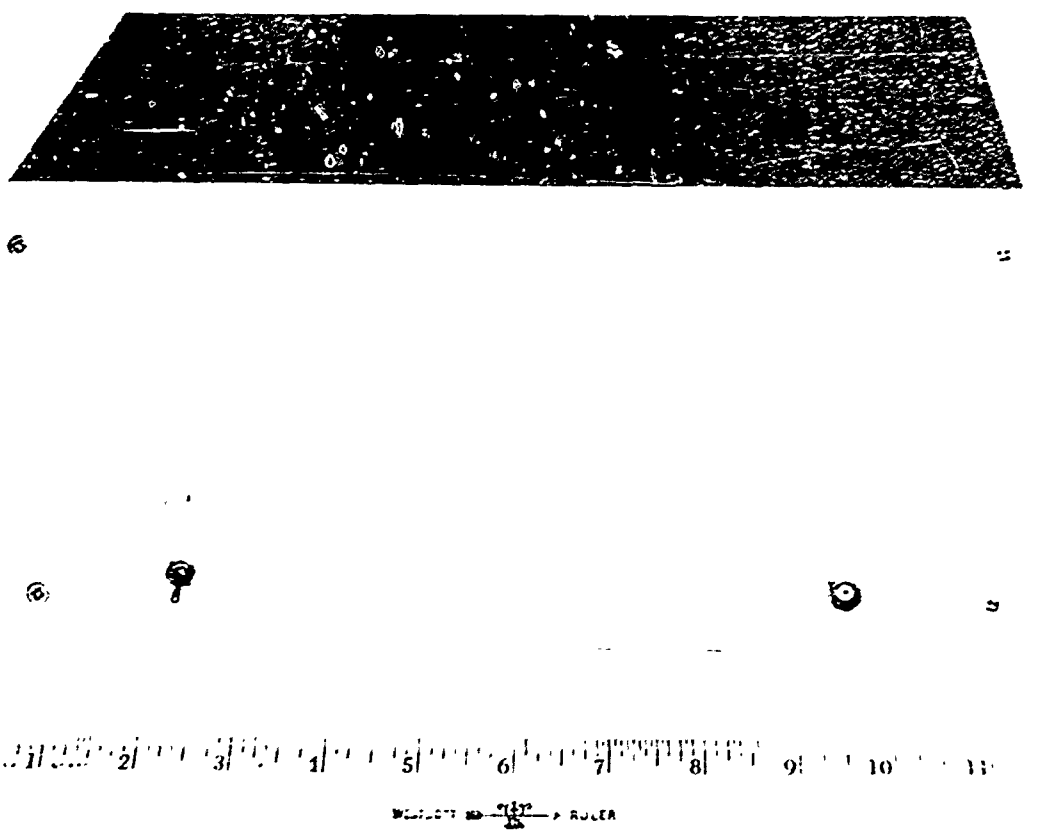

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Figure 28. Phase Coherency Test Set

accomplished as shown in Figure 29 by splitting the synthesizer No. 1 output into two identical components in a wideband power splitter and applying these two signals to the A and B inputs of the test set. The input signals to the double-balanced mixer (A_1 and B_1) and the reading on the true RMS voltmeter (E_o' RMS (MAX)) are recorded. After these readings are taken, the test set is fed from synthesizers No. 1 and No. 2 as shown in Figure 30. The mixer input and true RMS voltmeter readings A_2, B_2, and E_0' RMS are recorded. The RMS phase difference between synthesizer outputs is then given by the equation

$$\phi \text{ rms} = \sqrt{6 - \sqrt{36 - 24\left(1 - \left[\frac{A_1 B_1}{A_2 B_2}\right]\left[\frac{E_o' \text{ RMS}}{E_o' \text{ RMS (MAX)}}\right]\right)}} \text{ with}$$

ϕrms in radians. The same procedure is used for both Mode I and Mode II phase coherency measurements (see Appendix A).

In order to verify the accuracy of phase coherency measurements obtained using the above-mentioned equipment and procedures, an additional test was performed whereby a phase shift of one radian at 70 MHz was introduced in the test setup when synthesizer No. 1 was compared against itself. This was accomplished by adding a length of coaxial cable yielding approximately one radian of phase shift at 70 MHz between the power splitter and A channel input of the test set. Since the coax exhibits a linear phase shift vs. frequency characteristics, the phase shifts produced at 40, 50, and 60 MHz were 4/7 radian, 5/7 radian and 6/7 radian, respectively. Based on the average occurrence of 40, 50, 60, and 70-MHz S&TDL outputs in the frequency-hopping sequence (this is known since the frequency-hopping sequence is known), the RMS value of phase shift produced by the coaxial cable was calculated to be 0.7602 radians. Thus, an expected value of phase shift was available for comparison with values as determined by the phase coherency test set. (The coaxial cable was cut for 1 radian phase shift at 70 MHz. Measurements using a vector voltmeter indicated it actually produced a phase shift of 0.942 radians at 70 MHz. The measured values of phase shift produced by the cable at 40, 50, 60, and 70 MHz were used to calculate the expected phase shift of 0.7602 radians). The results of this experiment and of the general phase coherency measurements between synthesizers are included in the Test Results, Section VI.

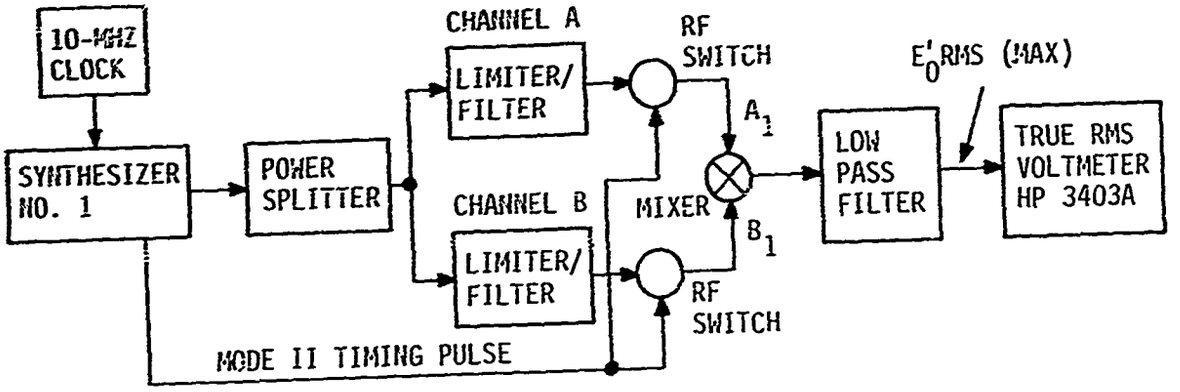


Figure 29. Phase Coherency Reference Signal Determination

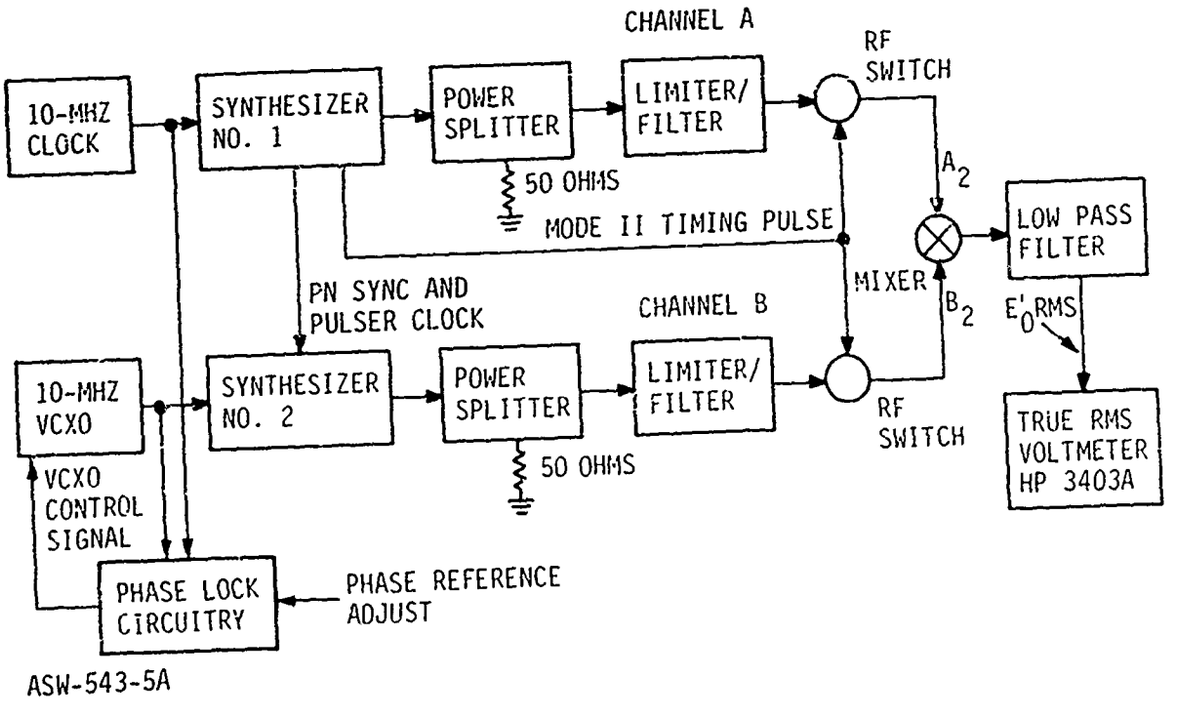


Figure 30. Phase Coherency Determination

SECTION VI

TEST RESULTS AND SYSTEM PERFORMANCE

1. OUTPUT WAVEFORMS

The following photographs illustrate some of the output waveforms produced by the synthesizers. Figure 31a is an oscillogram of the synthesizer outputs in Mode I operation and illustrates the continuous nature of the output signals. Figure 31b shows the output in Mode II operation and illustrates the 6-millisecond periodicity of the signals. Figure 32 shows a more detailed view of the 40, 50, 60, and 70 MHz outputs of the synthesizers. The biphase modulations representative of the 127-chip PN codes contained on each SWTDL become evident in this figure as is the near-constant amplitude of the signals. Figure 33 is a more detailed view of the synthesizer outputs in Mode II operation. In this oscillogram, the 40, 50, 60, and 70-MHz RF bursts are superimposed. Figure 34 shows the biphase modulation produced by the pseudo-random coding of a (60 MHz) SWTDL output transducer. Each PN chip is 100 nanoseconds long as a consequence of the 10 megabit/second PN chip rate inherent in the SWTDL design. Figure 35 illustrates the initial conditions on the 60-MHz PN code (the initial conditions for all four codes are the same). In this oscillogram, a 50-MHz burst has just ended and the 60-MHz burst is just beginning. Figure 36 illustrates several points in the frequency-hopping sequence where transitions from one frequency to another occur. As can be seen, the transitions are smooth and in most cases the change in frequency is quite apparent.

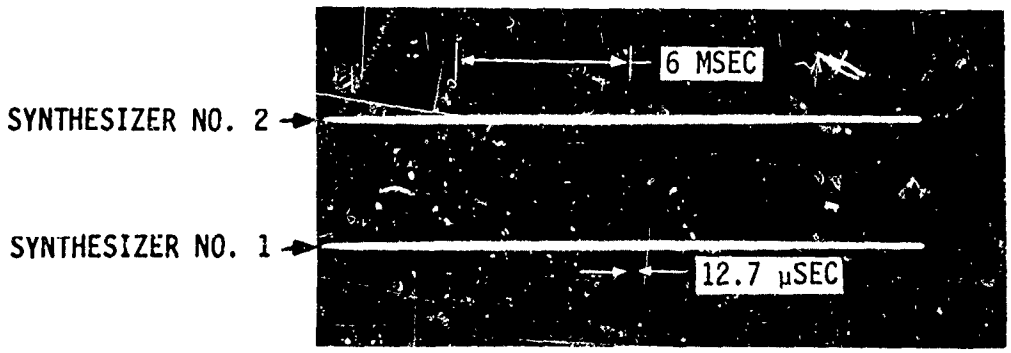
Figure 37a is a frequency domain representation of the synthesizer output displayed; 10-MHz per division in the horizontal axis and 10 dB per division on the vertical axis with the center of the spectrum centered at 55 MHz. The $(\sin x/x)^2$ shape of each SWTDL output is clearly evident as is the line structuring of the energy contained in the spectrum. Figure 37b is the same spectrum displayed at 5 MHz per horizontal division. Figure 37c is an individual display of the 50-MHz spectrum. The high-frequency side lobe of the $(\sin x/x)^2$ spectrum is slightly lower than the low-frequency side lobe because of the rolloff in pulser spectrum.

2. TEST RESULTS

A number of phase coherency measurements were made in order to determine the average value of phase coherency between synthesizers. The tests revealed an average departure from perfect phase coherency between synthesizers of 16 degrees RMS in Mode I operation and 18 degrees RMS in Mode II operation. The two parameters which had the most effect on attainable coherency were the SWTDL output matching network tuning and variations of the 5-volt supply voltages used by the synthesizer logic. Variations in SWTDL output matching network tuning affected coherency because of the nonlinear phase shift vs. frequency (i.e., dispersive) characteristics that resulted from mistuning the matching networks. Variations in 5-volt logic supply affected coherency because of variations in logic thresholds (and hence, in pulser clock time position) that occurred when the logic supply voltage was varied.

VERTICAL = 1 VOLT/CM
HORIZONTAL = 100 μSEC/CM

(a)



VERTICAL = 1 VOLT/CM
HORIZONTAL = 2 MSEC/CM

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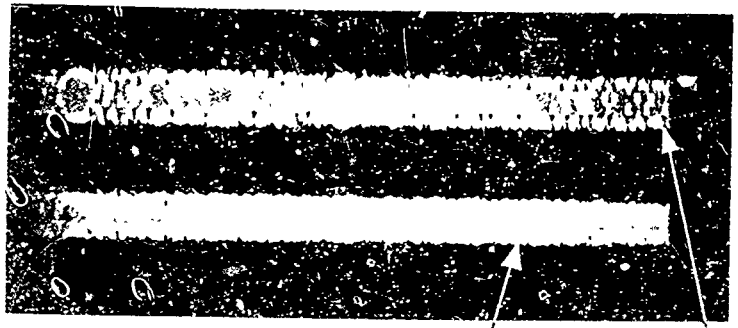
(b)

Figure 31. Synthesizer Output

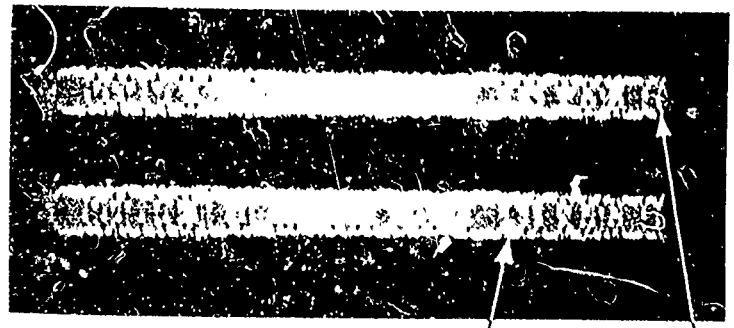


(a) 40 MHz

SYNTHESIZER NO. 1

SYNTHESIZER NO. 2

VERTICAL = 1 VOLT/CM
HORIZONTAL = 1.27 μSEC/CM



(b) 50 MHz

SYNTHESIZER NO. 1

SYNTHESIZER NO. 2

VERTICAL = 1 VOLT/CM
HORIZONTAL = 1.27 μSEC/CM

(c) 60 MHz

SYNTHESIZER NO. 1

SYNTHESIZER NO. 2

VERTICAL = 1 VOLT/CM
HORIZONTAL = 1.27 μSEC/CM

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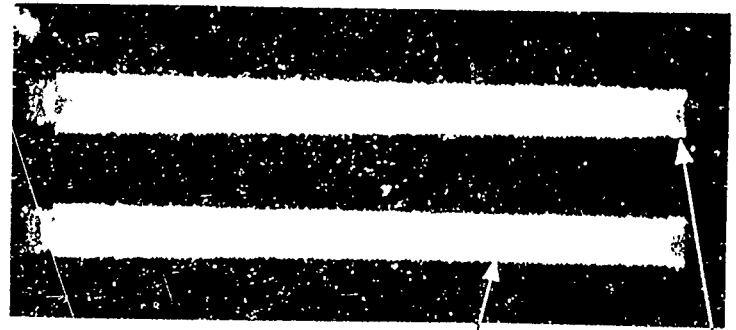


(d) 70 MHz

SYNTHESIZER NO. 1

SYNTHESIZER NO. 2

VERTICAL = 1 VOLT/CM
HORIZONTAL = 1.27 μSEC/CM

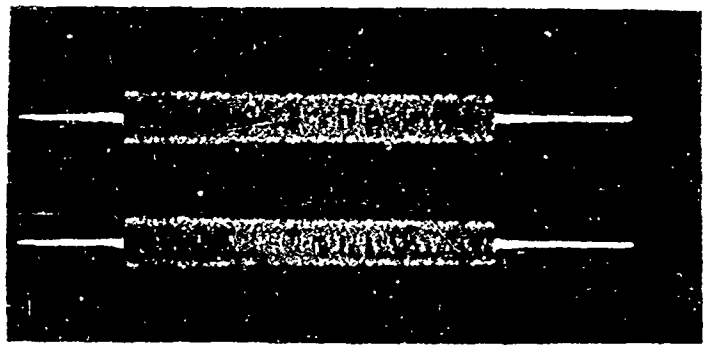


Figure 33. Superimposed Mode II Output

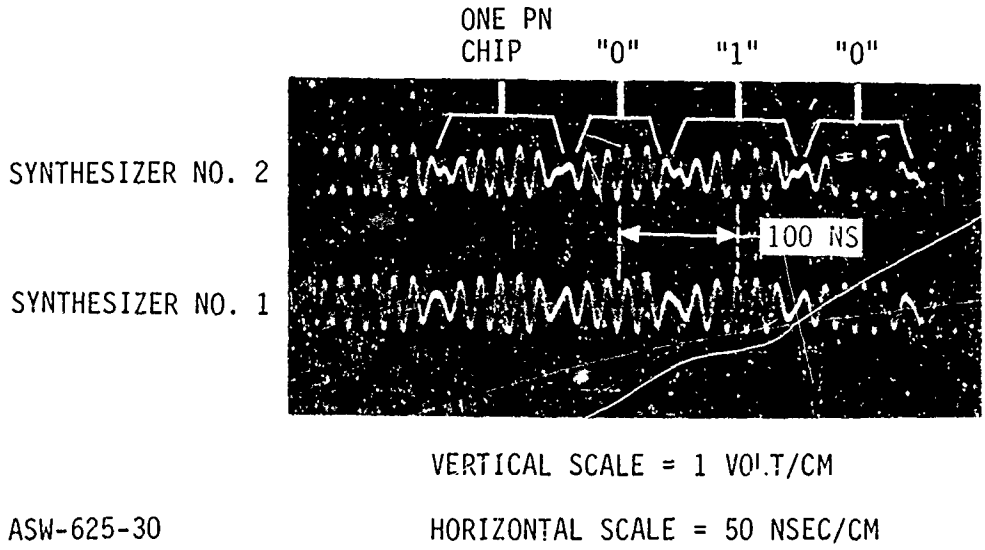


Figure 34. Biphase Modulation

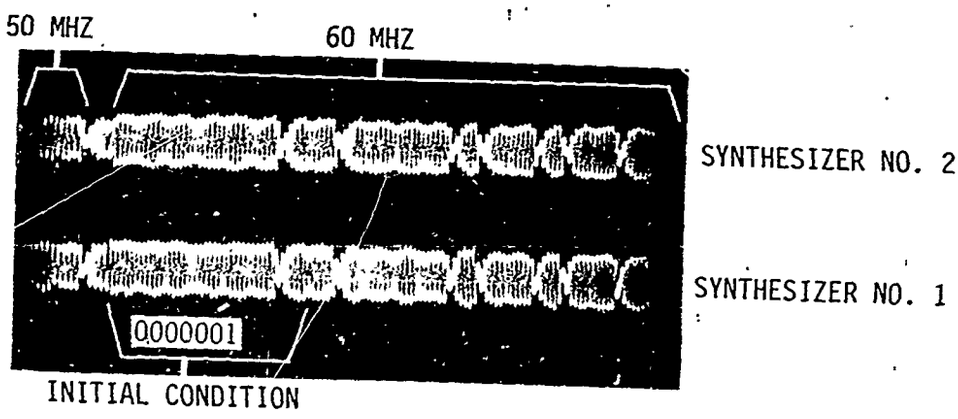
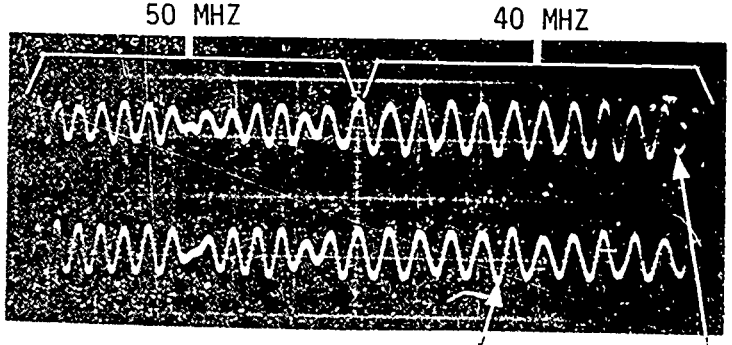
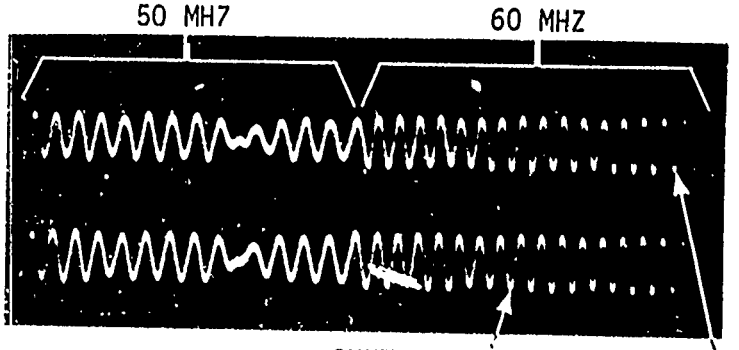


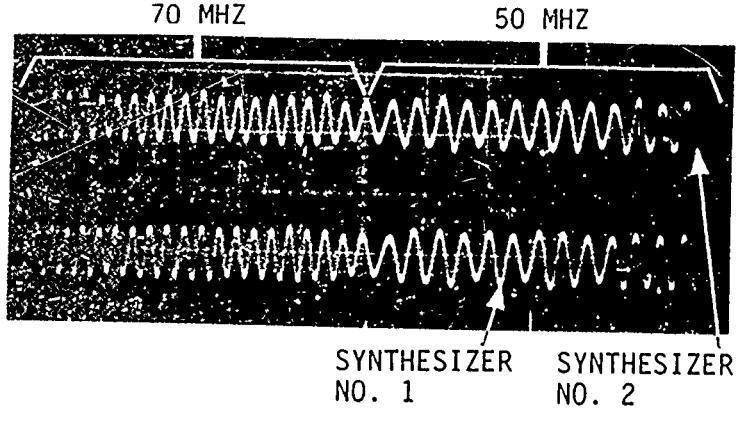
Figure 35. PN Code Initial Conditions



VERTICAL = 1 VOLT/CM
HORIZONTAL = 50 NSEC/CM

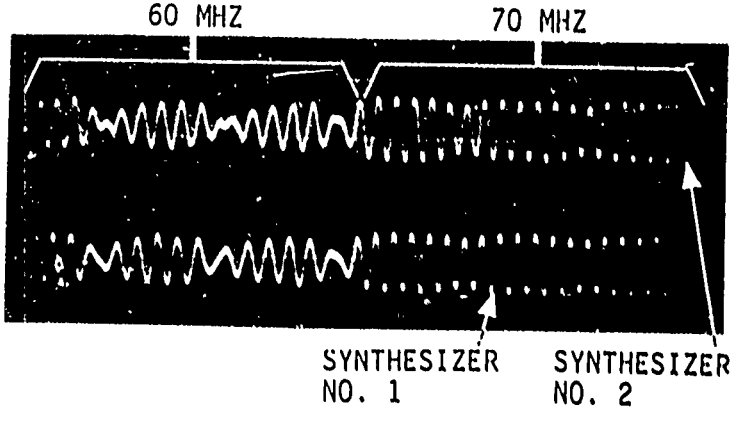


VERTICAL = 1 VOLT/CM
HORIZONTAL = 50 NSEC/CM

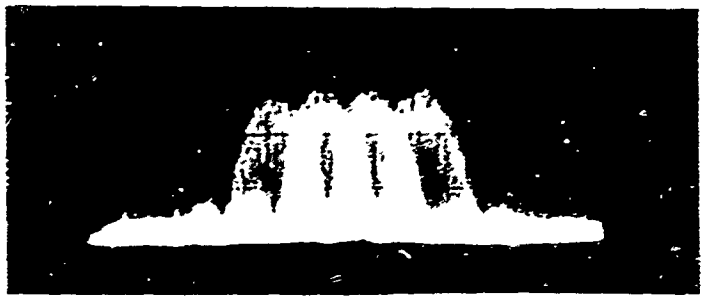


VERTICAL = 1 VOLT/CM
HORIZONTAL = 50 NSEC/CM

ASW-625-32

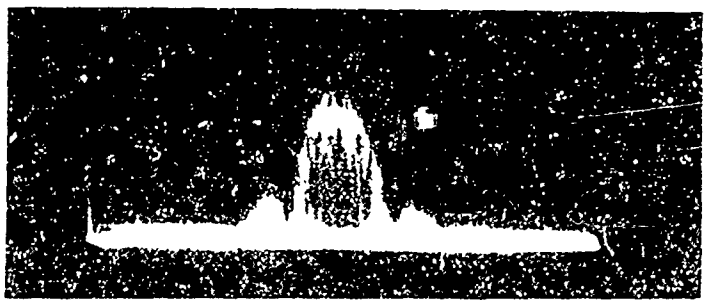


VERTICAL = 1 VOLT/CM
HORIZONTAL = 50 NSEC/CM



(a)

(b)



ASW-625-33 (c) 50 MHz

Figure 37. Synthesizer Frequency Spectrum

As would be expected, the most significant contribution to incoherency occurred during the 70-MHz segments of the frequency hopping sequence and the least significant contribution occurred during the 40-MHz segments. This effect can be seen in the oscillograms of Figures 38 and 39. Figure 38a is an oscillogram of the phase coherency test set phase error voltage (the signal measured by the true RMS voltmeter, see Figure 27). The top trace represents the error voltage produced when synthesizer No. 1 is split into two components with one component delaying one radian at 70 MHz as previously described. The bottom trace is the error voltage produced when synthesizer No. 1 is compared with synthesizer No. 2. The upper trace shows the variations in the dc level of the error voltage that occur as the synthesizer hops from one frequency to another. (A 0-volt error voltage level would represent a 90-degree phase relationship between test set input signals as the test set double-balanced mixer takes the cosine of the phase difference between input signals).

Figure 38b is a comparison of error voltages for synthesizer No. 1 compared with synthesizer No. 2, (upper trace), and of synthesizer No. 1 split into two identical (and theoretically perfectly coherent) components (lower trace). Figures 38a and 38b were taken in Mode I operation with the same time base and at the same point within the frequency-hopping sequence and thus, their horizontal axis correspond to the same points in time. Note in Figure 38b that the portions of the upper and lower traces corresponding to the 70-MHz segment are noticably different, while the 40, 50, and 60-MHz segments are nearly identical.

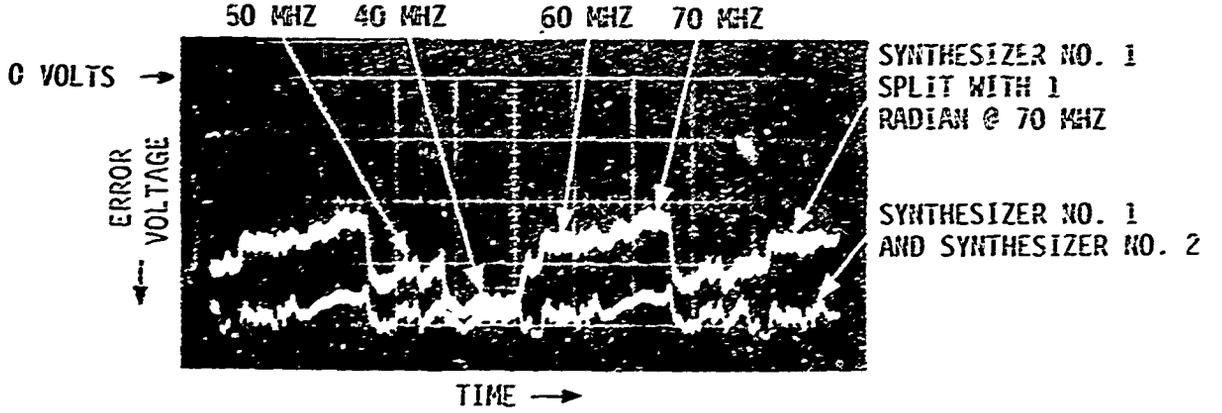
Figure 39 shows the error voltages in Mode II operation. The trace on the left in Figure 39a shows the superimposed error voltages for the 40, 50, 60, and 70 MHz segments when synthesizer No. 1 was split into two identical components. The trace on the right of Figure 39a shows the error voltages for synthesizer No. 1 split and the one radian phase shift at 70 MHz installed. The different error voltage levels for the 40, 50, 60, and 70-MHz segments are clearly evident.

Figure 39b shows the error voltages for synthesizer No. 1 split into two identical components (left trace) and synthesizer No. 1 compared with synthesizer No. 2 (right trace).

As mentioned previously, the one radian (at 70 MHz) phase shift coaxial cable was used to check the accuracy of the test set and test procedures. It theoretically should have provided an RMS phase incoherency of 0.7602 radians over the 40-MHz hopping bandwidth. In practice, RMS phase incoherences of about 0.776 radians were measured using the test cable which represents a difference of about 1 degree from the theoretical and measured values.

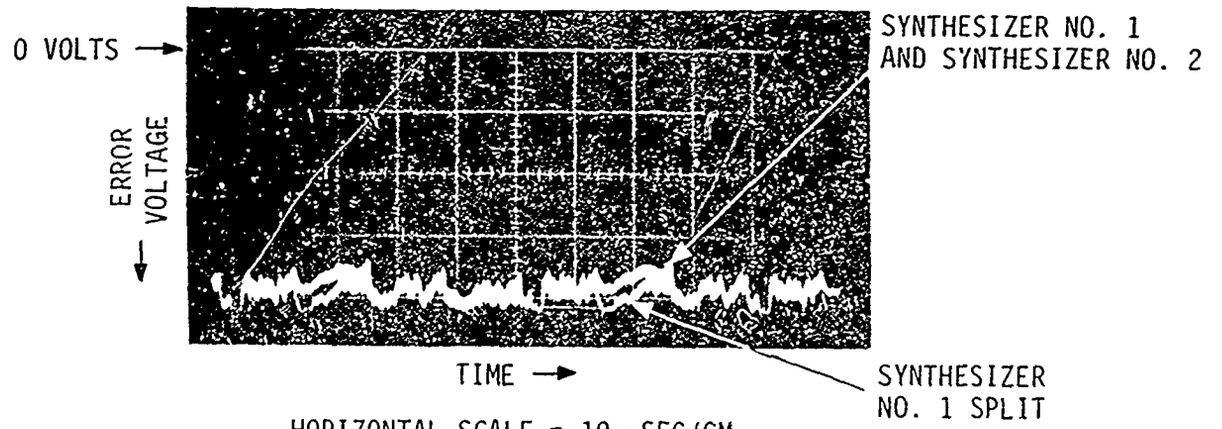
Additional testing was performed to determine the effect of temperature on synthesizer operating characteristics. For these tests, synthesizer No. 1 was placed in an environmental chamber, while synthesizer No. 2 and the coherency test set were kept in the ambient ($25^{o}C$) laboratory environment.

Synthesizer No. 1 was stabilized at $+55^{o}C$ and checks were made of synchronization circuit performance, signal output amplitude, and coherency. The output amplitude remained constant and no problems were encountered with either the pulser clock or PN synchronization circuits. A shift in phase between



HORIZONTAL SCALE = 10 μSEC/CM

(a)

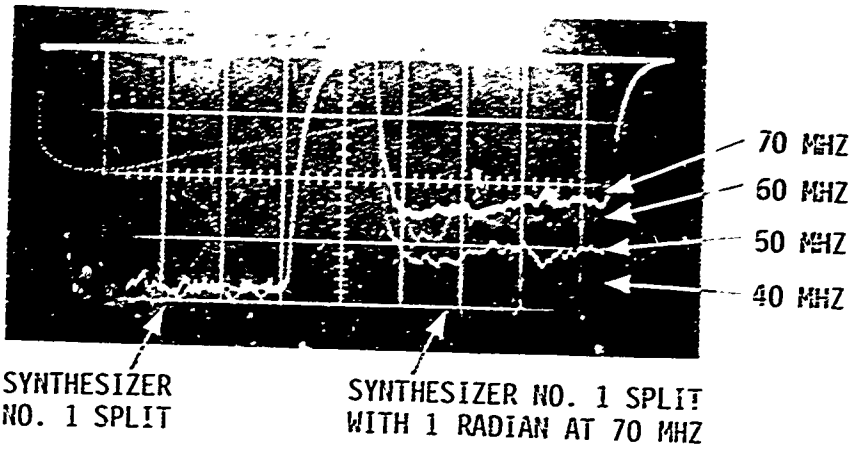


HORIZONTAL SCALE = 10 μSEC/CM

ASW-625-34

(b)

Figure 38. Mode I Coherency Error Signal



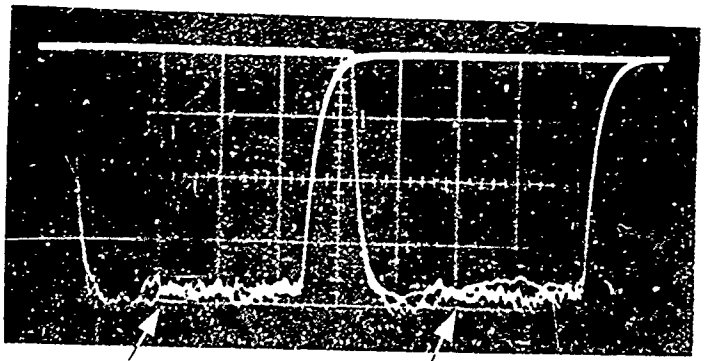


Figure 39. Mode II Coherency Error Signal

the 10-MHz clocks in synthesizer No. 1 and No. 2 occurred, but this was compensated by means of the "$\Delta\phi$" adjustment in the synthesizer No. 2 phase lock loop circuit. The variation in phase coherency between the 10-MHz clocks had been expected, because no attempt at temperature compensation was included in the 10-MHz clock synchronization circuitry design.

The measurements of phase incoherency between synthesizers indicated an incoherency of about 21 degrees RMS in Mode I operation and 22.5 degrees RMS in Mode II operation. This represented an average degradation of about 4.5 degrees RMS relative to the values of coherency obtained when both synthesizers were at ambient temperature. Based on the temperature coefficient of ST-Quartz and the operating characteristics of the synthesizers and coherency test set, the value of coherency degradation expected (due strictly to the 30°C temperature difference between synthesizers) was calculated to be approximately 3.7 degrees RMS.

Synthesizer No. 1 was then stabilized at 0°C and checks were again made of synchronization, output amplitude, and coherency. No problems were encountered with the synchronization circuitry (except for a readjustment of the relative phase of the 10-MHz clocks), and the output amplitude remained constant. The measurement of phase coherency between synthesizers indicated a degradation of about 1.5 degrees RMS in Modes I and II relative to the values obtained at ambient. This result corresponded reasonably well to a calculated degradation of 2.6 degrees RMS based upon a 25°C difference in temperature between synthesizers. The differences between measured and calculated coherency degradation are most likely due to the degree of measurement error possible with the phase coherency test set.

The conclusions drawn from the temperature tests were that (at least between 0°C and +55°C) the phase coherency between synthesizers was not seriously degraded and that the majority of the degradation was the result of the temperature difference between the surface wave devices.

3. COMPONENT FAILURES

During the course of system integration and testing, both synthesizers accumulated a considerable amount of operating time (a conservative estimate is 400 hours). During this time, the only component failure noted was the silver epoxy bonds used to fasten gold wires to the metalized pads of the surface wave device input and output transducers. In several instances, it was noted that a surface wave device output signal would become distorted and/or low in amplitude. In each case, the problem resulted from a high-ohmic resistance between the gold wire and the transducer metalization. Apparently, some type of oxidation process occurred which prevented a satisfactory electrical contact between the silver particles contained in the silver-epoxy adhesive and the gold wire or transducer metalization. In each case, the problem was solved by passing a small electric current through the epoxy bond by placing one probe of an ohmmeter on the gold wire and the other probe on the transducer pad metalization and switching to the high-resistance scale of the ohmmeter (a Simpson model 260 was used). Apparently, the ensuing flow of current would destroy the oxidation because in all cases, a low-ohmic resistance would then be achieved. This problem occurred in three separate SWTDL epoxy bonds during the course of system fabrication, but once corrected, no additional problems appeared.

SECTION VII
FUTURE WORK AND RECOMMENDATIONS

1. FUTURE WORK

Based upon the results achieved to date on synthesizer performance, it has been decided to expand the capabilities of one of the synthesizers such that it will produce a coherent frequency-hopped waveform of 100-MHz bandwidth. The modified synthesizer will employ seven surface wave devices and will generate a waveform covering a frequency range from 55 MHz to 155 MHz. This synthesizer will have the capability of phase shift key modulating the waveform with binary data at either 2249 bits/second or at 10 megabits/second. In addition, the synthesizer will have the capability of producing a 100-MHz pseudo-randomly hopped waveform or a sequentially hopped waveform whose bandwidth can be varied from 10 MHz to 100 MHz in seven increments.

Associated with the modified synthesizer will be a data synchronizer that will be capable of dehopping the synthesizer output waveform, matched filter detecting the dehopped pseudo-noise signal, demodulating the signal and reconstructing the 2249-bit/second (or 10 megabits/second) information orginated at the synthesizer. The data synchronizer will employ surface wave devices as parallel correlating matched filters and a surface wave device re-entry delay line for coherent predetection integration when in the 2249-bit/second data mode. The data synchronizer will also employ a surface wave device local oscillator injection synthesizer to translate the incoming frequency-hopped signal to a common processing signal frequency.

2. RECOMMENDATIONS

The 40-MHz bandwidth FH/PN synthesizer development described in this report demonstrates the feasibility of employing surface wave devices for coherent FH/PN waveform generation. In the context of the equipment performance achieved to date, certain recommendations can be made regarding future development efforts on these specific (40-MHz bandwidth) equipments.

a. Filtering

Bandpass filtering to restrict the spectrum occupancy of each individual SWTDL can be incorporated into the SWTDL transducer design. This is an important and necessary requirement of a FH/PN synthesizer (no matter how implemented) intended for use in a wideband communications system operating in a multiuser environment. Bandpass filtering with surface wave devices is a natural application of their characteristics and much development work has been performed recently both by Magnavox and other surface wave technology houses.

b. Offset Quadriphase Modulation

The use of offset quadriphase modulation of the synthesizer waveform should be considered in view of the reduced spectrum splatter it can

provide in a practical FH/PN multiuser system. (A discussion of spectrum splatter in relation to various shift key modulation techniques is presented in Appendix B.) As pointed out in Appendix B, the effect of communications channel nonlinearities can restore the spectrum splatter in pretransmission filtered biphase and conventional quadriphase modulated signals. Offset quadriphase modulation can reduce this effect and can be implemented in the design of the SWTDL transducers.

c. Code Diversity

A criticism occasionally raised regarding the use of surface wave devices for the generation of PN modulated waveforms is the lack of PN code diversity provided, since the PN code generating surface wave device patterns are normally fixed. This is not necessarily true, however, since recent developments in the technology demonstrate that programmable tap surface wave devices are feasible and in fact have been built. If the need for programmable tap devices truly becomes a system requirement in a practical application, the technology required to provide this versatility exists and can be applied.

d. Multifunction SWTDL's

The four SWTDL signal generators used in each synthesizer were fabricated on separate quartz substrates. This was done mainly for convenience since the synthesizers were a breadboard development. In a more practical application, the four SWTDL's could be fabricated on a common SWTDL substrate thus affording a significant savings in space. If this were done, it is possible that the four output transducers could be summed on the SWTDL substrate, thus eliminating the need for the power combiner required in the present design. The bandpass filtering, offset quadriphase modulation and switchable tap devices previously described could, of course, also be incorporated at the same time.

e. Synthesizer Logic

The digital logic used in the synthesizer breadboards is composed entirely of discrete dual in-line TTL devices. A large portion of this logic could have been implemented using a low-speed, low-power consumption logic type such as COSMOS. TTL is a high-speed logic family and needs only to be used in specific portions of the synthesizers, such as in the SWTDL pulser circuits and the higher operating speed portions of the frequency-divider circuits. In addition to the use of a lower speed logic family, the majority of the logic could be fabricated using medium or large-scale integration in order to significantly reduce the amount of physical volume and interdevice wiring required.

APPENDIX A

MATHEMATICAL ANALYSIS OF PHASE COHERENCY MEASUREMENT

This analysis is based on the phase coherency test setups described in Section V of this report.

Let the output from Synthesizer No. 1 after passing through a perfect limiter/filter be given by:

$$E_1(t) = A(t) \cos(\omega t)$$

Let the output from Synthesizer No. 2 after passing through a perfect limiter/filter be given by the following equation.

$$E_2(t) = A(t) \cos(\omega t + \phi(t))$$

where: $A(t)$ = the amplitude of each synthesizer output after limiting. $A(t)$ has a constant magnitude $|A|$ and a polarity determined by the phase reversals of the SWTDL maximal length sequence codes. Consequently, $A(t) = \pm|A|$.

ω = the radian frequency of each synthesizer output.

$\phi(t)$ = the instantaneous phase difference between Synthesizer No. 1 and Synthesizer No. 2 outputs. Note that $\phi(t)$ is comprised of two components: A deterministic component results from variations between corresponding surface wave tapped delay lines in each synthesizer and by differences in the RF pulsers and other RF portions of the two synthesizers. A random component results from the effect of the thermal noise associated with each synthesizer output.

A perfect limiter is assumed -- a limiter that produces a constant amplitude output signal regardless of the amplitude or frequency of the input signal. Measurements of synthesizer performance utilizing practical limiters is discussed later in this appendix.

The synthesizer outputs $E_1(t)$ and $E_2(t)$ are multiplied in a double balanced mixer and produce a resultant output voltage $E_0(t)$, where

$$E_0(t) = K\, A(t) \cos(\omega t) A(t) \cos(\omega t + \phi(t))$$

$E_0(t)$ can also be written as

$$E_0(t) = \frac{K A^2(t)}{2} [\cos (2\omega t + \phi(t)) + \cos (\phi(t))]$$

K = the gain of the mixer in volts/(volt)^2.

The mixer output $E_0(t)$ is fed through a lowpass filter with cutoff frequency ω_c. Since the highest output frequency of the synthesizer is centered at 70 MHz and will have significant spectral components extending to 75 MHz, the filter will cutoff at approximately 75 MHz.

The output of the lowpass filter, $E_0'(t)$, is then

$$E_0'(t) = \frac{K A^2(t)}{2} [\cos (\phi(t))]$$

$E_0'(t)$ is a measure of the instantaneous phase difference between Synthesizers No. 1 and No. 2. The signal $E_0'(t)$ is fed to a true rms voltmeter which measures the true rms value of

$$\frac{K A^2(t)}{2} [\cos (\phi(t))]$$

Note that

$$A^2(t) = [\pm|A|]^2 = A^2$$

Therefore,

$$E_0'(t) - \frac{K A^2}{2} [\cos (\phi(t))]$$

$\cos (\phi(t))$ can be expressed by the series expansion

$$\cos (\phi(t)) = 1 - \frac{\phi^2(t)}{2!} + \frac{\phi^4(t)}{4!} - \ldots (-1)^N \left(\frac{\phi^{2N}(t)}{2N!}\right)$$

N = 0, 1, 2, ..., $\phi(t)$ in radians.

For small $\phi(t)$, the series can be truncated to

$$\cos \phi(t) \cong 1 - \frac{\phi^2(t)}{2!} + \frac{\phi^4(t)}{4!}$$

Hence, $E_0'(t)$ can be expressed as

$$E_0'(t) \cong \frac{K A^2}{2} \left[1 - \frac{\phi^2(t)}{2!} + \frac{\phi^4(t)}{4!}\right]$$

Some mathematical manipulation of the preceding equation results in the following

$$\frac{2E_0'(t)}{K A^2} = E_0''(t) = 1 - \frac{\phi^2(t)}{2!} + \frac{\phi^4(t)}{4!}$$

$$\frac{\phi^4(t)}{4!} - \frac{\phi^2(t)}{2!} + 1 - E_0''(t) = 0$$

$$\phi^4(t) - 12\phi^2(t) + 24[1 - E_0''(t)] = 0$$

Let $z(t) = \phi^2(t)$, then the preceding equation becomes

$$z^2(t) - 12\, z(t) + 24[1 - E_0''(t)] = 0$$

Applying the quadratic formula to the preceding equation results in

$$z(t) = 6 - \sqrt{36 - 24(1 - E_0''(t))}$$

Hence,

$$\phi(t) = \sqrt{z(t)} = \sqrt{6 - \sqrt{36 - 24(1 - E_0''(t)}} \quad \text{radians}$$

Now

$$E_0''(t) = \frac{2E_0'(t)}{K A^2}$$

and the true rms voltmeter measures E_0'rms. But

$$E_0''\text{rms} = \frac{2E_0'\text{rms}}{K A^2}$$

Since the input signals to the mixer are $A(t) \cos(\omega t)$ and $A(t) \cos(\omega t + \phi(t))$, their rms values are

$$A_{rms} = \frac{A}{\sqrt{2}}$$

But

$$A^2_{rms} = \frac{A^2}{2}$$

Therefore,

$$E_0''rms = \frac{E_0'rms}{K\,A^2rms}$$

and

$$\phi rms = \sqrt{6 - \sqrt{36 - 24\left[1 - \frac{E_0'rms}{K\,A^2rms}\right]}} \quad \text{radians.}$$

If the output from one synthesizer is split into two equal amplitude phase coherent components in a wideband power splitter, and the two components are limited, filtered, and fed to the mixer, the resultant voltage indicated on the true rms voltmeter can be used as a calibration voltage for the system. The resultant voltage, $E_0'rms$ (max), represents an rms phase angle ϕ(rms) of zero, since the two components are phase coherent. $E_0'rms$ (max) equals $K\,A^2rms$, since for ϕ(rms) = 0 the term

$$\frac{E_0'rms}{K\,A^2rms}$$

in the equation for ϕ(rms) must equal unity. Therefore, ϕ(rms) can be written as

$$\phi(rms) = \sqrt{6 - \sqrt{36 - 24\left[1 - \frac{E_0'rms}{E_0'rms\ (max)}\right]}} \quad \text{radians}$$

The analysis used to derive the analytical expression for ϕ(rms) assumed the use of perfect limiters in making the measurements of $E_0'rms$ (max) and $E_0'rms$. In practice, perfect limiter performance is not obtained and allowances must be made for this non-perfect limiter operation. These allowances involve a minor modification of the expression for synthesizer phase coherency, ϕ(rms), and may be derived as follows.

The calibration signal or reference reading $E_0'rms$ (max) can be expressed as

$$E_0'rms\ (max) = A_1B_1K \cos \phi_1(t)$$

where

A_1 and B_1 = the amplitudes of the imperfectly limited signals fed to the double balanced mixer in the phase coherency test circuit (rms values)

K = the mixer gain constant

$\phi_1(t)$ = the phase difference between mixer input signals.

Likewise, $E_0'rms$ is given by

$$E_0'rms = A_2B_2K \cos \phi_2(t)$$

where

A_2 and B_2 = the mixer input signal amplitudes (rms values)

$\phi_2(t)$ = the phase difference between mixer input signals.

Note that for the reference reading $E_0'rms$ (max) the phase difference between mixer input signals is zero, hence $\phi_1(t) = 0$. For the measurement of $E_0'rms$, however, $\phi_2(t)$ represents the phase difference (i.e., the measure of coherency) between synthesizers. By dividing $E_0'rms$ by $E_0'rms$ (max) , we obtain the relationship

$$\frac{E_0'rms}{E_0'rms\ (max)} = \frac{A_2B_2K \cos \phi_2(t)}{A_1B_1K \cos \phi_1(t)} = \frac{A_2B_2 \cos \phi_2(t)}{A_1{}^3{}_1}$$

since $\phi_1(t) = 0$

Therefore

$$\text{Cos } \phi_2(t) = \left[\frac{E_0'rms}{E_0'rms\ (max)}\right]\left[\frac{A_1B_1}{A_2B_2}\right]$$

If we expand $\text{Cos } \phi_2(t)$ in a power series and solve for ϕ_2 as was done before for the case of perfect limiter operation, we obtain an expression for $\phi(rms)$ as

$$\phi(rms) = \sqrt{6 - \sqrt{36 - 24\left[1 - \left(\frac{A_1B_1}{A_2B_2}\right)\left(\frac{E_0'rms}{E_0'rms\ (max)}\right)\right]}} \quad \text{radians}$$

A comparison of this equation with the previously derived equation for $\phi(rms)$ reveals that it is identical in form but contains the correction factor $(A_1B_1)/(A_2B_2)$ which accounts for non-perfect limiter operation. Note that if the limiter operation were perfect,

$$\frac{A_1B_1}{A_2B_2} = 1$$

and the equation reduces to the previously derived equation for $\phi(rms)$ assuming perfect limiter operation.

APPENDIX B

SPECTRUM SPLATTER FROM PHASE SHIFT KEY MODULATION

A practical application of the frequency-hopping concept to a communications system is a configuration where a large number of users require simultaneous use of the communications channel. To make such a system efficient in terms of bandwidth, requires that each frequency slot within the channel bandwidth is used at all times. Thus, a possible system configuration might be one where the N slots available are occupied by transmissions from N users. The frequency slot assignments of the N users are permuted in a manner such that no more than one user occupies the same frequency slot at the same time, i.e., the frequency-hopping sequences of the N users are orthogonal. (Time division multiplex could be employed in addition to the frequency division multiplexing to allow more than N system users). The orthogonality of frequency slot assignments is the key to the previously mentioned systems multiuser capability and therefore, the effects of spectrum splatter within the channel is important.

The biphase PN modulation contained on the output waveform of the synthesizers described in this report causes each frequency burst to have a $\left(\frac{\sin x}{x}\right)^2$ spectrum centered about the particular burst center frequency. Energy from any one burst splatters over the entire operating bandwidth of the synthesizer. This spectrum splatter could cause cochannel interference in an otherwise perfectly coordinated time and frequency orthogonal system. This is especially troublesome when the system must operate with multiuser signals whose strengths vary over a large dynamic range.

Filtering of the $\left(\frac{\sin x}{x}\right)^2$ spectrum of each frequency burst prior to transmission is effective in reducing the effect of spectrum splatter if tha channel is linear. However, in the nonlinear channel environment, the out-of-band power in the filtered $\left(\frac{\sin x}{x}\right)^2$ spectrum is restored (this is the practical situation when one considers the use of typical high power transmitters, limiters in satellite or airborne repeaters, etc.). If hard limiting is encountered, the original $\left(\frac{\sin x}{x}\right)^2$ spectrum is totally restored for biphase modulation and is essentially restored for normal quadriphase modulation.

There is a technique using quadriphase modulation, however, that considerably reduces the degree to which the out-of-band power is restored by hard limiting. The technique employs independent biphase modulations on the sine and cosine components offset from one another by half a bit. Therefore, only $\pm \pi/2$ transitions can occur. Since the modulations on the quadrature components are independent, the resulting spectrum before filtering has the power spectral density of biphase modulation at the actual symbol rate. When the normal biphase modulation is filtered, the amplitude of the signal goes through zero when a transition of π degrees is made. With the technique just

described, however, the amplitude of the signal never reduces to a level below -0.707 times the full envelope amplitude and, thus, subsequent effects of limiting are reduced.

The specific levels of out-of-band spectrum occupancy produced by this system have been evaluated by digital computation. The results are summarized for one particular case in Figure B-1. These results are quite striking. At a frequency which is eight times the bit rate, the filtered and hard limited signal using this offset technique is 80 dB below the $\left(\frac{\sin x}{x}\right)^2$ spectrum. This simple technique, therefore, is very powerful in suppressing out-of-band spectral noise and should be considered for use to reduce spectrum splatter in a frequency-hopping system.

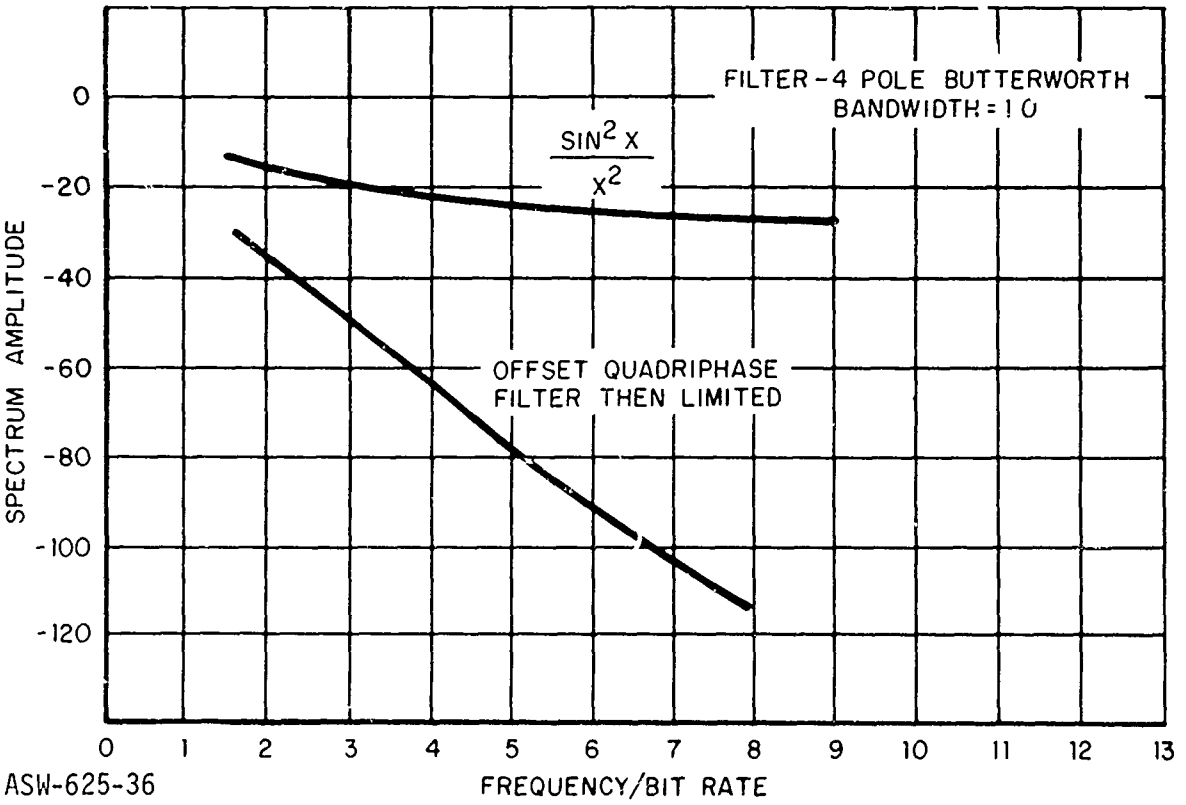


Figure B-1. Spectrum Splatter for Offset Quadriphase Modulation